1. The pipelined execution of instructions is difficult due to:
a) speculative calculations
b) branching
c) true dependence
d) unconditional jumps
e) anti-dependency

2. The optimization methods for pipeline instruction execution are:
a) multiple streams
b) changing the order of fetching instructions
c) instruction window

3. The branch prediction method is:
a) nested branch
b) procedural dependency elimination
c) branch history table
d) register window

4. Renaming of registers enables:
a) elimination of the true dependency
b) elimination of the output dependency
c) elimination of anti-dependency
d) elimination of procedural dependency

5. The features of RISC processors are:
a) low numer of registers
b) large cache size
c) instructions executed in one cycle
d) complex control unit
e) fixed length of instructions

6. The features of CISC processors are:
a) instructions executed in one cycle
b) no operations on data from memory
c) long list of instructions
d) complex control unit

7. The registers window enables:
a) minimization of accesses to memory
b) minimization of registers used
c) elimination of dependencies in the data flow
d) efficient transfer of parameters to subroutines

8. The idea of RISC is supported by:
a) semantic gap
b) shorter programs
c) small number of arguments of procedures

d) poor use of complex instructions

9. The methods of increasing the efficiency of superscalar processing are:
a) loop buffer
b) reordering of instructions
c) register windows

10. The anti-dependency of R1 and R2 instructions occurs when:
a) the result of R1 is used in R2
b) the results of R1 and R2 are stored in the same place
c) the argument of R1 is changed by R2
d) R1 and R2 use the same register

11. The resource access conflict in superscalar processing can be eliminated by:
a) renaming registers
b) changing the order of fetching instructions
c) changing the order of executing instructions
d) changing the order of completing instructions
e) duplicating resources

12. The instruction window enables:
a) elimination of the true dependency
b) elimination of anti-dependency
c) separation of the decoding and execution steps
d) out-of-order execution

13. One control unit have architecture
a) SIMD
b) MIMD
c) MISD
d) SISD

14. Many processing units have architectures:
a) SIMD
b) MIMD
c) MISD
d) SISD

15. Cache consistency issue affects certain architectures like:
a) SISD architectures
b) MIMD architectures
c) SIMD architectures

16. Distributed memory is used in architectures:
a) SISD
b) MIMD
c) Any

17. Features of the SMP architecture are:
a) distributed organization memory
b) processors with comparable capabilities
c) integrated operating system

18. Possible cluster organizations are:
a) servers with common operational memory
b) common system bus
c) servers connected to disks
d) separate servers

19. The MESI protocol ensures cache consistency by:
a) directory of blocks placed in the cache
b) write with update
c) storing the block state in the cache
d) write with invalidate
e) write-through

20. The NUMA architecture features include:
a) no cache
b) each processor has its own cache
c) each processor has access to the cache of other processors
d) memory blocks are copied to local memory
e) each processor has access to the same memory

21. Organizations of multi-core processors differ in:
a) I / O system
b) cache organization
c) main memory organization
d) homogeneity / diversity of cores.

22. The metrics used for computer performance evaluation is:
a) MHz
b) FLOPS
c) MB / s
d) SPECspeed

23. Applications that effectively use the computing power of multi-core processors are:
a) multithreaded applications
b) computing oriented applications
c) Java applications
d) web applications
e) word processors

24. Solutions that increase the performance of a computer system include:
a) parallel processing

b) shared bus
c) memory protection
d) cache
e) shared memory

25. Prefetch is:
a) fetching the instruction before the previous instruction is completed
b) Parallel download of several instructions.
c) fetching an instruction to the cache