Projektowanie Systemów Wbudowanych mgr inż. Leszek Ciopiński Laboratorium 1.: Szybki start.



Х

WYBRAĆ "CREATE A NEW PROJECT"

### 💐 New Project Wizard

## Introduction

The New Project Wizard helps you create a new project and preliminary project settings, including the following:

- Project name and directory
- Name of the top-level design entity
- Project files and libraries
- Target device family and device
- EDA tool settings

You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.

Don't show me this introduction again

< Back

Einish

Next >

Cancel

Help

## 💐 New Project Wizard

## Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

C:/Documents and Settings/Leszek/Pulpit/q\_lab1

What is the name of this project?

lab1	
Use Existing Project Settings	
	< <u>Back</u> <u>Next</u> > <u>Finish</u> Cancel <u>H</u> elp

×

[...]

## 🍓 New Project Wizard

## Add Files [page 2 of 5]

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.

jie name:	<u>A</u> dd
File Name Type Library Design Entry/Synthesis Tool HDL Version	Add All
	Remove
	Up
	Down
	Properties
recify the path names of any non-default libraries. User Libraries	
pecify the path names of any non-default libraries. User Libraries	

## Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family	Show in 'Available devices' list					
Eamily: Cyclone II	Pac <u>k</u> age:	Any				
Devices: All	Pin <u>c</u> ount:	Any				
Target device	Sp <u>e</u> ed grade:	Any				
Auto device selected by the Fitter	Name filter:	ep2c35f672c6				
Specific device selected in 'Available devices' list	Show adva	anced devices 🗌 HardCopy compatible only 🔒				
O Other: n/a						

### Available devices:

Glob	PLL	s	dded multiplier 9-bit elements		Memory Bit	User I/Os	LEs	Core Voltage	Name
16	4	4		70	483840	475	33216	1.2V	P2C35F672C6
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Help		ancel	ext > <u>F</u> inish Cano	ack	< <u>B</u>				
		ancel	ext > Einish Cano	ack	< <u>B</u>				

## EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

### EDA tools:

Tool Type	Tool Name		Format(s)		Run Tool Automatically
Design Entry/Synthesis	<none></none>	*	<none></none>	V	Run this tool automatically to synthesize the current design
Simulation	<none></none>	*	<none></none>	Y	Run gate-level simulation automatically after compilation
Formal Verification	<none></none>	*			
Board-Level	Timing		<none></none>	~	
	Symbol		<none></none>	~	
1	Signal Integrity		<none></none>	~	
	Boundary Scan		<none></none>	~	

< <u>B</u>ack

 $\underline{N}ext >$ 

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Cancel

Help

## Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:	C:/Documents and Settings/Leszek/Pulpit/q_lab1
Project name:	lab1
Top-level design entity:	lab 1
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Family name:	Cyclone II
Device:	EP2C35F672C6
EDA tools:	
Design entry/synthesis:	<none> (<none>)</none></none>
Simulation:	<none> (<none>)</none></none>
Timing analysis:	0
Operating conditions:	
Core voltage:	1.2V
Junction temperature range:	0-85 ℃

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Cancel

Help

# Następnie wywołujemy

- \* File | New ... => Block Diagram / Shematic File
- \* File | Save As ... => nazwa projektu
- \* Assigments | Pin Planner
- \* Assigments | Import Assigments => wybrać plik "DE2\_piny.qsf"
- \* Otworzyć Pin Planner



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oject Navigator 무료 ×	lab1.bdf
tity	
Cyclone II: EP2C35F672C6	
Hierarchy 📄 Files 🖓 Design Units 🔂 R(\)	
ks 무준×	Paste
Customize	Delete
	Undate Symbol or Block
Task 🔘	
Compile Design	Show
🛨 🏲 Analysis & Synthesis	Insert Symbol
Assembler (Generate programming files)	€ Zoom In Ctrl+Space Symbol as Block
🕀 🕨 TimeQuest Timing Analysis	Zoom Out Ctrl+Shift+Space
🗄 🕨 EDA Netlist Writer	Zoom
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(System (I)) (Processing)	308, 192, 0%, 00
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## 🔡 Symbol





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Flow: Compilation Customize		
Task () Compile Design Analysis & Synthesis Etter (Place & Boute)		
Assembler (Generate programming files)     FimeQuest Timing Analysis     EDA Netlist Writer		
Program Device (Open Programmer)		
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# Do wykonania

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Skopiować wejścia i połączyć

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🔔 Hardware Setup.	No Hardware			Mode:	JTAG		~	Progress:			
Enable real-time IS	P to allow background progr	amming (for MAX II and	MAX V devices)								
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Add Device											
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<b>WYBRA</b>	Ć TOOL	PROG	RAMN	IER_							

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USB-Blaster		Local	USB-0	[Barris Hard

🐌 Programmer - C	:/Documents and Settin	ngs/Leszek/Pulpit	/q_lab1/lab1 -	lab1 - [output	t_files/lab1.	cdf]						
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## **DODAJEMY PROCESOR**

**NIOS II WERSJA II/E** 

gatore altera_up_avalon_sram	(	Documentation
Show signals Show signals	valon_sram	

### 🛔 Qsys

<u>File Edit System View Tools H</u>elp



### 📕 Qsys

<u>File Edit System View Tools H</u> elp									
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🔍 itan wart 🛛 🗶 🕂	Use	Connections	Name	Description		Export	Clock	Base	
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3 "Reset vector memory" (resetSlave)	(None)	out of range. Valid ran	ges: [sram.avalon_sram_slave	:sram.avalon_sram_s	System.nios2_cpu_	qsys			
Strain Content in the second s	onSlav	e) (None) out of range.	Valid ranges: [sram.avalon_sra	am_slave:sram.avalor	System.nios2_cpu_	qsys			_
Reset slave is not specified. Please selec	t the rea	set slave			System.nios2_cpu_	qsys			~
8 Errors, 1 Warning				-1	* ** ***				

	K		
* Block Diagram	Configurations		
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external_interfaceconduit	Expansion Header:	GPIO 0 (JP1)	
altera_up_avalon_pa	arallel_port		
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## Parallel Port - parallel\_port\_0

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MegaCore'	altera_u

Diagram		
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A Qsys									
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Project Wew Component Library B-Bridges Clock and Reset Configuration & Programming DSP E-Embedded Processors C-Interface Protocols C-Memories and Memory Contro		×	data_master     data_master     instruction_master     itag_debug_module_re     jtag_debug_module     custom_instruction_m     El zeear	Avalon Memory M Avalon Memory M Reset Output Avalon Memory M Custom Instruction	apped Master apped Master apped Slave n Master	Double-click to export Double-click to export Double-click to export Double-click to export Double-click to export	[cik] [cik] [cik] [cik]	• 0x0000_08	
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⊕ Communications ⊟ Generic IO — ● DE0-Nano ADC C — ● Parallel Port		•	+ +	→ clock_reset → clock_reset_reset → avalon_parallel_port_s external_interface	Clock Input Reset Input . Avalon Memory M Conduit	apped Slave	Double-click to export Double-click to export Double-click to export red_led_external_interfa	zegar [clock_reset] [clock_reset]	✓ 0x0000_00
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12 Errors, 1 Warning									~

Nios II Processor - n	rios2_cpu_qsys						
gacore altera_nios2_q	sys						Documentation
Block Diagram						Dynamic Branch Predicti	ion 🦉
Show signals			Memory Usage (e.g Stratix IV) Two M	9Ks (or equiv.)	Two M9Ks + cache	Three M9Ks + cache	
	nios2_cpu_qsys		Thardware Arithmetic Operation				
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			Exception Vector				
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			T MMU and MPU				
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			Only include the MMU using an operating	system that explicitly su	pports an MMU.		

Cancel

Finish

## **POPRAWA PARAMETRÓW NIOS-A**

UZUPEŁNIENIE RESET VECTOR MEMORY I EXCEPTION VECTOR MEMORY

×	+	Description	Export	Clock	Base	End	IRQ Tags
ject Wew Component rary Bridges Clock and Reset Configuration & Programming DSP		ios II Processor lock Input eset Input valon Memory Mapped Master valon Memory Mapped Master eset Output valon Memory Mapped Slave	Double-click to export Double-click to export Double-click to export Double-click to export Double-click to export Double-click to export	<b>zegar</b> [clk] [clk] [clk] [clk] [clk]	II @ 0x0000_0800	RQ 0 IRC 0x0000_0fff	2 31
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	Pa	arallel Port lock Input	Double-click to export	zegar			

Description	Path	<u>k</u>
B Errors		~
itag_uart.avalon_jtag_slave (0x00x7) overlaps sram.avalon_sram_slave (0x00x7ffff)	System.nios2_cpu_qsys.data_master	=
red_LED.avalon_parallel_port_slave (0x00xf) overlaps jtag_uart.avalon_jtag_slave (0x00x7)	System.nios2_cpu_qsys.data_master	
Switches.avalon_parallel_port_slave (0x00xf) overlaps red_LED.avalon_parallel_port_slave (0x00xf)	System.nios2_cpu_qsys.data_master	
		V

## PODŁĄCZAMY SYGNAŁ PRZERWANIA

### 🛔 Qsys



Name       Inios2_cpu_qsys       clk       reset_n       data_master       instruction_master       jtag_debug_module       custom_instruction_m.       E     zegar       clk_in       clk_in       clk_instruction_m.       E     zegar       clk_in       clk_instruction_m.       E     zegar       clk_instruction_m.       E     zegar       clk_instruction_m.       Clk_instruction_m.       E     jtag_ur       clk_reset       E     sram       clock_reset_reset       clock_reset_reset       clk       reset       avalon_sram_slave       E     jtag_uart       clk       reset       avalon_itag_slave       E     red_LED       clock_reset	Description           Nios II Processor           Clock Input           Reset Input           Avaion Memory Mapped Master           Avaion Memory Mapped Master           Avaion Memory Mapped Master           Avaion Memory Mapped Master           Avaion Memory Mapped Slave           Custom Instruction Master           Clock Source           Clock Noute           Clock Output           Reset Input           Clock Output           Reset Output           SRAM/SSRAM Controller           Clock Input           Reset Input           Conduit           Avaion Memory Mapped Slave           JTAG UART           Clock Input           Reset Input           Conduit           Avaion Memory Mapped Slave           JTAG UART           Clock Input           Reset Input           Avaion Memory Mapped Slave           Javaion Memory Mapped Slave           Parallel Port	Export	Clock  Zegar [clk] Zegar [clock_reset] [clock_reset] [clock_reset] Zegar [clk] [clk] [clk] [clk]	Base • 0x0010_0800
<ul> <li>nios2_cpu_qsys</li> <li>clk</li> <li>reset_n</li> <li>data_master</li> <li>instruction_master</li> <li>jtag_debug_module_ree</li> <li>jtag_debug_module</li> <li>custom_instruction_m.</li> <li>zegar</li> <li>clk_in</li> <li>clk_in_reset</li> <li>clk</li> <li>clk_reset</li> <li>sram</li> <li>clock_reset_reset</li> <li>clock_reset_reset</li> <li>clock_reset_reset</li> <li>clock_reset_reset</li> <li>clk</li> <li>reset_avalon_sram_slave</li> <li>jtag_uart</li> <li>clk</li> <li>reset</li> <li>avalon_itag_slave</li> <li>red_LED</li> <li>clock_reset</li> </ul>	Nios II Processor           Clock Input           Reset Input           Avalon Memory Mapped Master           Avalon Memory Mapped Master           Avalon Memory Mapped Master           Avalon Memory Mapped Master           Clock Input           Avalon Memory Mapped Slave           Custom Instruction Master           Clock Source           Clock Noute           Clock Output           Reset Input           Clock Output           Reset Output           SRAM/SSRAM Controller           Clock Input           Reset Input           Conduit           Avalon Memory Mapped Slave           JTAG UART           Clock Input           Reset Input           Avalon Memory Mapped Slave           JTAG UART           Clock Input           Reset Input           Avalon Memory Mapped Slave           Parallel Port	Double-click to export         Double-click to export	zegar [clk] [clk] [clk] [clk] [clk] [clk] zegar [clck_reset] [clock_reset] zegar [clock_reset] [clk]	<ul> <li>0x0010_0800</li> <li>0x0008_0000</li> </ul>
<pre>clk reset_n data_master instruction_master jtag_debug_module_re jtag_debug_module custom_instruction_m.  Zegar clk_in clk_in_reset clk clk clk_reset Sram clock_reset clock_reset clock_reset clock_reset clock_reset clk reset avalon_sram_slave i itag_uart clk reset avalon_itag_slave i red_LED clock_reset</pre>	Clock Input Reset Input Avalon Memory Mapped Master Avalon Memory Mapped Master Reset Output Avalon Memory Mapped Slave Custom Instruction Master Clock Source Clock Source Clock Input Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export         Double-click to export	zegar [clk] [clk] [clk] [clk] [clk] [clk] zegar [clock_reset] [clock_reset] zegar [clock_reset] zegar	<ul> <li>0x0010_0800</li> <li>0x0008_0000</li> <li>0x0010_1020</li> </ul>
<pre>reset_n data_master instruction_master itag_debug_module_rei itag_debug_module custom_instruction_m.</pre>	Reset Input Avaion Memory Mapped Master Avaion Memory Mapped Master Reset Output Avaion Memory Mapped Slave Custom Instruction Master Clock Source Clock Source Clock Input Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avaion Memory Mapped Slave JTAG UART Clock Input Reset Input Avaion Memory Mapped Slave Parallel Port	Double-click to export	[clk] [clk] [clk] [clk] [clk] [clk] zegar [clock_reset] [clock_reset] zegar [clk] [clk]	<ul> <li>0x0010_0800</li> <li>0x0008_0000</li> <li>0x0010_1020</li> </ul>
data_master         instruction_master         jtag_debug_module_rei         jtag_debug_module         custom_instruction_m.         l       zegar         clk_in         clk_in         clk_inset         clk_inset         clk_ingeset         interface         avalon_sram_slave         interface         avalon_itag_slave         clk_ingeset         clk_ingeset         clk_ingeset         clk_ingeset         clk_ingeset <td< td=""><td>Avalon Memory Mapped Master Avalon Memory Mapped Master  Reset Output Avalon Memory Mapped Slave Custom Instruction Master Clock Source Clock Input Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port</td><td>Double-click to export         Double-click to export</td><td>[clk] [clk] [clk] [clk] [clk] zegar [clock_reset] [clock_reset] zegar [clk] [clk]</td><td><ul> <li>0x0010_0800</li> <li>0x0008_0000</li> <li>0x0010_1020</li> </ul></td></td<>	Avalon Memory Mapped Master Avalon Memory Mapped Master  Reset Output Avalon Memory Mapped Slave Custom Instruction Master Clock Source Clock Input Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export	[clk] [clk] [clk] [clk] [clk] zegar [clock_reset] [clock_reset] zegar [clk] [clk]	<ul> <li>0x0010_0800</li> <li>0x0008_0000</li> <li>0x0010_1020</li> </ul>
<pre>instruction_master jtag_debug_module_rei jtag_debug_module custom_instruction_m.</pre>	Avalon Memory Mapped Master Reset Output Avalon Memory Mapped Slave Custom Instruction Master Clock Source Clock Input Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export	[clk] [clk] [clk] zegar zegar [clock_reset] [clock_reset] zegar [clk] [clk]	<ul> <li>0x0010_0800</li> <li>0x0008_0000</li> <li>0x0010_1020</li> </ul>
<pre>itag_debug_module_rei itag_debug_module custom_instruction_m. custom_instruction_m. clk_in clk_in clk_in clk_reset clk clk clk_reset clock_reset clock_reset clock_reset clock_reset clock_reset clk clk reset clk</pre>	Reset Output     Avalon Memory Mapped Slave     Custom Instruction Master     Clock Source     Clock Input     Reset Input     Clock Output     Reset Output     SRAM/SSRAM Controller     Clock Input     Reset Input     Conduit     Avalon Memory Mapped Slave     JTAG UART     Clock Input     Reset Input     Avalon Memory Mapped Slave     Parallel Port	Double-click to export	[clk] [clk] zegar zegar [clock_reset] [clock_reset] zegar [clk] [clk]	<ul> <li>0x0010_0800</li> <li>0x0008_0000</li> <li>0x0010_1020</li> </ul>
<pre>&gt;</pre>	Avalon Memory Mapped Slave Custom Instruction Master Clock Source Clock Input Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export         Double-click to export         clk         reset         Double-click to export	[clk] zegar zegar [clock_reset] [clock_reset] zegar [clk] [clk]	<ul> <li>0x0010_0800</li> <li>0x0008_0000</li> <li>0x0010_1020</li> </ul>
<ul> <li>custom_instruction_m.</li> <li>zegar         <ul> <li>clk_in</li> <li>clk_in_reset</li> <li>clk</li> <li>clk_reset</li> <li>sram</li> <li>clock_reset_reset</li> <li>clock_reset_reset</li> <li>external_interface</li> <li>avalon_sram_slave</li> <li>jtag_uart</li> <li>clk</li> <li>reset</li> <li>avalon_itag_slave</li> <li>red_LED</li> <li>clock_reset</li> </ul> </li> </ul>	Custom Instruction Master     Clock Source     Clock Input     Reset Input     Clock Output     Reset Output     SRAM/SSRAM Controller     Clock Input     Reset Input     Conduit     Avalon Memory Mapped Slave     JTAG UART     Clock Input     Reset Input     Avalon Memory Mapped Slave     Parallel Port	Double-click to export         clk         reset         Double-click to export	zegar zegar [clock_reset] [clock_reset] zegar [clk] [clk]	0x0008_0000
<ul> <li>□ zegar clk_in clk_in_reset clk clk_reset</li> <li>□ sram clock_reset clock_reset clock_reset_reset external_interface avalon_sram_slave</li> <li>□ jtag_uart clk reset avalon_itag_slave</li> <li>□ red_LED clock_reset</li> </ul>	Clock Source Clock Input Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	clk reset Double-click to export Double-click to export Double-click to export sram_external_interface Double-click to export Double-click to export Double-click to export Double-click to export Double-click to export	zegar zegar [clock_reset] [clock_reset] zegar [clk] [clk]	0x0008_0000
<pre>clk_in clk_in_reset clk clk_clk_reset clk clk_reset clock_reset</pre>	Clock Input Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	clk reset Double-click to export Double-click to export Double-click to export Sram_external_interface Double-click to export	zegar zegar [clock_reset] [clock_reset] zegar [clk] [clk]	© 0x0008_0000
<pre>clk_in_reset clk clk_clk_reset clk clk_reset clock_reset clock_reset clock_reset external_interface avalon_sram_slave iftag_uart clk reset avalon_itag_slave clock_reset</pre>	Reset Input Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	reset Double-click to export Double-click to export Double-click to export Sram_external_interface Double-click to export	zegar zegar [clock_reset] [clock_reset] zegar [clk] [clk]	© 0x0008_0000
<pre>clk clk_reset clock_reset clock_reset clock_reset clock_reset clock_reset clock_reset clock_reset clock_reset clock_reset clk reset avalon_sram_slave clk reset avalon_itag_slave clck_reset clock_reset</pre>	Clock Output Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export Double-click to export Double-click to export sram_external_interface Double-click to export Double-click to export Double-click to export Double-click to export	zegar zegar [clock_reset] [clock_reset] zegar [clk] [clk]	© 0x0008_0000
<pre>clk_reset clock_reset clock_reset clock_reset clock_reset clock_reset clock_reset clock_reset clock_reset clock_reset clk reset avalon_stag_slave clk reset avalon_itag_slave clck_reset</pre>	Reset Output SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export Double-click to export Sram_external_interface Double-click to export	zegar [clock_reset] [clock_reset] zegar [clk] [clk]	• 0x0008_0000
	SRAM/SSRAM Controller Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export Double-click to export sram_external_interface Double-click to export Double-click to export Double-click to export Double-click to export	zegar [clock_reset] [clock_reset] zegar [clk] [clk]	■ 0x0008_0000
<pre>clock_reset clock_reset_reset external_interface avalon_sram_slave if itag_uart clk reset avalon_itag_slave ired_LED clock_reset</pre>	Clock Input Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export Double-click to export sram_external_interface Double-click to export Double-click to export Double-click to export Double-click to export	zegar [clock_reset] [clock_reset] zegar [clk] [clk]	■ 0x0008_0000
<pre>clock_reset_reset external_interface avalon_sram_slave i jtag_uart clk reset avalon_itag_slave i red_LED clock_reset</pre>	Reset Input Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export sram_external_interface Double-click to export Double-click to export Double-click to export Double-click to export	[clock_reset] [clock_reset] zegar [clk] [clk]	■ 0x0008_0000
<pre>external_interface avalon_sram_slave i jtag_uart clk reset avalon_itag_slave i red_LED clock_reset</pre>	Conduit Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	sram_external_interface Double-click to export Double-click to export Double-click to export Double-click to export	[clock_reset] zegar [clk] [clk]	■ 0x0008_0000
→ avalon_sram_slave ⇒ jtag_uart clk reset avalon_itag_slave ⇒ red_LED clock_reset	Avalon Memory Mapped Slave JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export Double-click to export Double-click to export Double-click to export	[clock_reset] zegar [clk] [clk]	■ 0x0008_0000
	JTAG UART Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export Double-click to export Double-click to export	zegar [clk] [clk]	- 0×0010 1020
	Clock Input Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export Double-click to export Double-click to export	zegar [clk] [clk]	0-0-010 1020
→ reset avalon_itag_slave □ red_LED clock_reset	Reset Input Avalon Memory Mapped Slave Parallel Port	Double-click to export Double-click to export	[clk] [clk]	- 0×0010 1020
avalon_itag_slave	Avalon Memory Mapped Slave Parallel Port	Double-click to export	[clk]	- 0x0010 1020
☐ red_LED clock_reset	Parallel Port	a second a second as any second	T. must	000010 1020
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	Avalon Memory Manned Slave	Double click to export	[clock_reset]	.0∞0010_1010
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el switches	Cleak leavet	Double allals to success		
clock_reset	Clock input	Double-click to export	zegar	
clock_reset_reset	Reset Input	Double-click to export	[clock_reset]	
zegar.clk reset				
	Path			
	external_interface switches clock_reset clock_reset zegar.clk_reset	external_interface       Conduit         external_interface       Parallel Port         clock_reset       Clock Input         clock_reset_reset       Reset Input         zegar.clk_reset       Path	external_interface       Conduit       red_led_external_interfa.         Parallel Port       Parallel Port         clock_reset       Clock Input         clock_reset_reset       Reset Input         zegar.clk_reset       Path	external_interface       Conduit       red_led_external_interfa         B switches       Parallel Port       Double-click to export       zegar         clock_reset       Clock Input       Double-click to export       zegar         clock_reset_reset       Reset Input       Double-click to export       [clock_reset]         zegar.clk_reset       Path

## PRZYPISYWANIE ADRESÓW BAZOWYCH

**SYSTEM I ASSIGN BASE ADDRESSES** 

<u>File E</u> dit <u>S</u> ystem <u>V</u> iew <u>T</u> ools <u>H</u> elp		
Component Library	System Contents Address Map Clo	ck Settings Project Settings Instance Parameters System Inspector HDL Example Generation
Component Library	System Contents Address Map Clo Simulation Create simulation model: Create testbench Qsys system: Create testbench simulation model: Synthesis Create HDL design files for sy Create block symbol file (.bsf) Output Directory Path: Simulation: Testbench: Synthesis: Generate	ckck Settings Project Settings     Verliog     Image: Instance Parameters     System Inspector     HDL Example     Verliog     Image: Instance Parameters     System Inspector     HDL Example     Verliog     Image: Instance Parameters     System Inspector     HDL Example     Verliog     Image: Instance Parameters     System Inspector     Image: Instance Parameters     Verliog     Image: Instance Parameters     Image: Instance Parameters     Verliog     Image: Instance Parameters <
Messages		
Description		Path
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Memory will be initialized from memor	ry.hex	System.memory

## **JAKO CREATE SIMULATION MODEL WYBIERAMY VERILOG**

WERSJA VHDL NIE JEST DOPRACOWANA W QUARTUSIE 12.1SP1

## 👪 Generate Completed



Stop

Info: Reusing file C:/altera\_testy/lab1b/moj\_system/synthesis/submodules/altera\_mer
Info: rsp\_xbar\_mux\_001: "moj\_system" instantiated altera\_merlin\_multiplexer "rsp\_xba
Info: Reusing file C:/altera\_testy/lab1b/moj\_system/synthesis/submodules/altera\_mer
Info: width\_adapter: "moj\_system" instantiated altera\_merlin\_width\_adapter "width\_ac
Info: Reusing file C:/altera\_testy/lab1b/moj\_system/synthesis/submodules/altera\_mer
Info: Reusing file C:/altera\_testy/lab1b/moj\_system/synthesis/submodules/altera\_mer
Info: Reusing file C:/altera\_testy/lab1b/moj\_system/synthesis/submodules/altera\_mer
Info: Reusing file C:/altera\_testy/lab1b/moj\_system/synthesis/submodules/altera\_mer
Info: req\_mapper: "moj\_system" instantiated altera\_irq\_mapper "irq\_mapper"
Info: moj\_system: Done moj\_system" with 26 modules, 72 files, 1400784 bytes
Info: ip-generate succeeded.

Info: Finished: Create HDL design files for synthesis

Generate Completed. 0 Errors, 0 Warnings

\_ 0 X 🕷 Quartus II 32-bit - C:/altera\_testy/lab1b/lab1 - lab1 Search altera.com 🖉 Settings - lab1 1 B 5 Project Navigator Category: Device... Files Files General lab1.bdf Files 4 Libraries Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the Operating Settings and Conditions project. Voltage Temperature Eile name: Add Compilation Process Settings Early Timing Estimate File Name Library Design Entry/Synthesis Tool HDL Version Type Add All Incremental Compilation Physical Synthesis Optimizations **Osys System File** <None> moj s... EDA Tool Settings moj\_s... Component Declaration File <None> Remove lab1.bdf Block Diagram/Schematic File <None> Design Entry/Synthesis Simulation Up A Hierarchy Files Desid Formal Verification Board-Level Down Tasks Analysis & Synthesis Settings VHDL Input Flow: Compilation Properties Verilog HDL Input Default Parameters LEDG[8..0] Task Fitter Settings TimeQuest Timing Analyzer 😑 🕨 Compile Design Assembler Design Assistant 🗄 🕨 Analysis & Synthesis SignalTap II Logic Analyzer 🗉 🕨 Fitter (Place & Route) Logic Analyzer Interface 🛨 🕨 Assembler (Generate PowerPlay Power Analyzer Settings SSN Analyzer ¢ > х 8 9 All 1 Ð Д Type ID Message > W Buy Software OK Cancel Apply Help System / Processing 287, 295 0% 00:00:00 🔞 🖉 🕘 🚳 🥘 関 an632.pdf (Obiekt ... 🛃 Start 🚞 3 Eksplorator Win... 🦉 bez tytułu - Paint 👗 Qsys - moj\_system.... 👿 🔊 23:19 💞 Quartus II 32-bit - .. 🖉 Settings - lab 1 NALEŻY DODAĆ PLIKI NOWEGO PODSYSTEMU

NAJWAŻNIEJSZY JEST PLIK TYPU QSYS SYSTEM FILE

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TW/OR7	VMV SVMR	NUN IL	VFGO	DUUC	<b>STEM</b>			

## **UWAGA: W PODSYSTEMIE WYSTĘPUJĄ:** INPUT (WEJŚCIE, NA NIEBIESKO), OUTPUT (WYJŚCIE, NA FIOLETOWO) I BIDIR (DWUKIERUNKOWE, NA ZIELONO)





Kolejne kroki

- \* Wykonać pełną kompilację
- \* Zaprogramować układ FPGA
- Wybrać polecenie menu Quartusa: Tools | Nios II Software Build Tools for Eclipse

# Nios II IDE

Quartus II	🖨 Nios II - Eclipse									
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Target hardware information SOPC Information File name: CPU name:	C: \altera_testy \ab 1b \moj_system.sopcinfo nios2_cpu_qsys	
Application project		
Project name: hello		
Project template Templates Blank Project	Template description Hello World prints 'Hello from Nios II' to STDOUT.	
Templates Blank Project Board Diagnostics	Template description Hello World prints 'Hello from Nios II' to STDOUT.	
Hello Freestanding Hello MicroC/OS-II Hello World	requires an STDOUT device in your system's hardware.	
Hello World Small Memory Test Memory Test Small Simple Socket Server	readme.txt file in the project directory. The BSP for this template is based on the Altera HAL operating system.	
Simple Socket Server (RGM Web Server Web Server (RGMII)	II) For information about how this software example relates to Nios II hardware design examples, refer to the Design Examples page of the Nios II documentation available with your installation at: <installation_directory>/nios2eds/documents/index.htm.</installation_directory>	

Nios II Application and BSP from Template		
Nios II Software Examples Select a board support package for your application		
<ul> <li>Create a new BSP project based on the application project template</li> </ul>		
Project name: hello_bsp		
Use default location		
Project location: C:\altera_testy\ab 1b\software\hello_bsp		
O Select an existing BSP project from your workspace		
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### Nios II - hello/hello world.c - Eclipse File Edit Source Refactor Navigate Search Run Project Nigs II Window Help 🛅 • 🔄 📴 🕒 🗎 🗄 🖞 🎯 • 🞯 • 🞯 • 🛛 🏇 • 🔘 • 💁 🖕 🥔 • 🖉 • 🖉 🖉 • 🖉 • 🖉 • 🖉 • 🖉 Nios II C/C++ - D 🗄 Outline 🖾 PD ello\_world.c - -🎦 Project Explorer 🛛 🔪 □ 🔄 🖢 ▽ 💱 🎼 😿 🔏 🖉 🗰 🔻 🗸 \* "Hello World" example. 🖃 😂 hello stdio.h 🗄 👯 Binaries main() : int \* This example prints 'Hello from Nios II' to the STDOUT strea E D Includes \* the Nios II 'standard', 'full featured', 'fast', and 'low cc 🗄 🥟 obi \* designs. It runs with or without the MicroC/OS-II RTOS and r 🗄 🚺 hello world.c \* device in your system's hardware. ⊞ ☆ hello.elf - [alteranios2/le] \* The memory footprint of this hosted application is ~69 kbyte create-this-app \* using the standard reference design. hello.map hello.objdump \* For a reduced footprint version of this template, and an exp 💧 Makefile \* to reduce the memory footprint for a given application, see readme.txt \* "small hello world" template. 🗄 😂 hello\_bsp [moj\_system] \*/ #include <stdio.h> int main() printf("Hello from Nios II!\n"); return 0; 3 < > 🖹 Problems 🧔 Tasks 📮 Console 🔲 Properties 🛗 Nios II Console 🔀 hello Nios II Hardware configuration - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: itaguart 0 Hello from Nios II!

# Dodajemy kod

- \* alt\_up\_parallel\_port\_dev\* ledr;\* alt\_up\_parallel\_port\_dev\* switches;
- \* ledr = alt\_up\_parallel\_port\_open\_dev
   (RED\_LED\_NAME);
- \* switches = alt\_up\_parallel\_port\_open\_dev
  (SWITCHES\_NAME);
- \* tmp = alt\_up\_parallel\_port\_read\_data(switches); \* alt\_up\_parallel\_port\_write\_data(ledr, tmp);



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