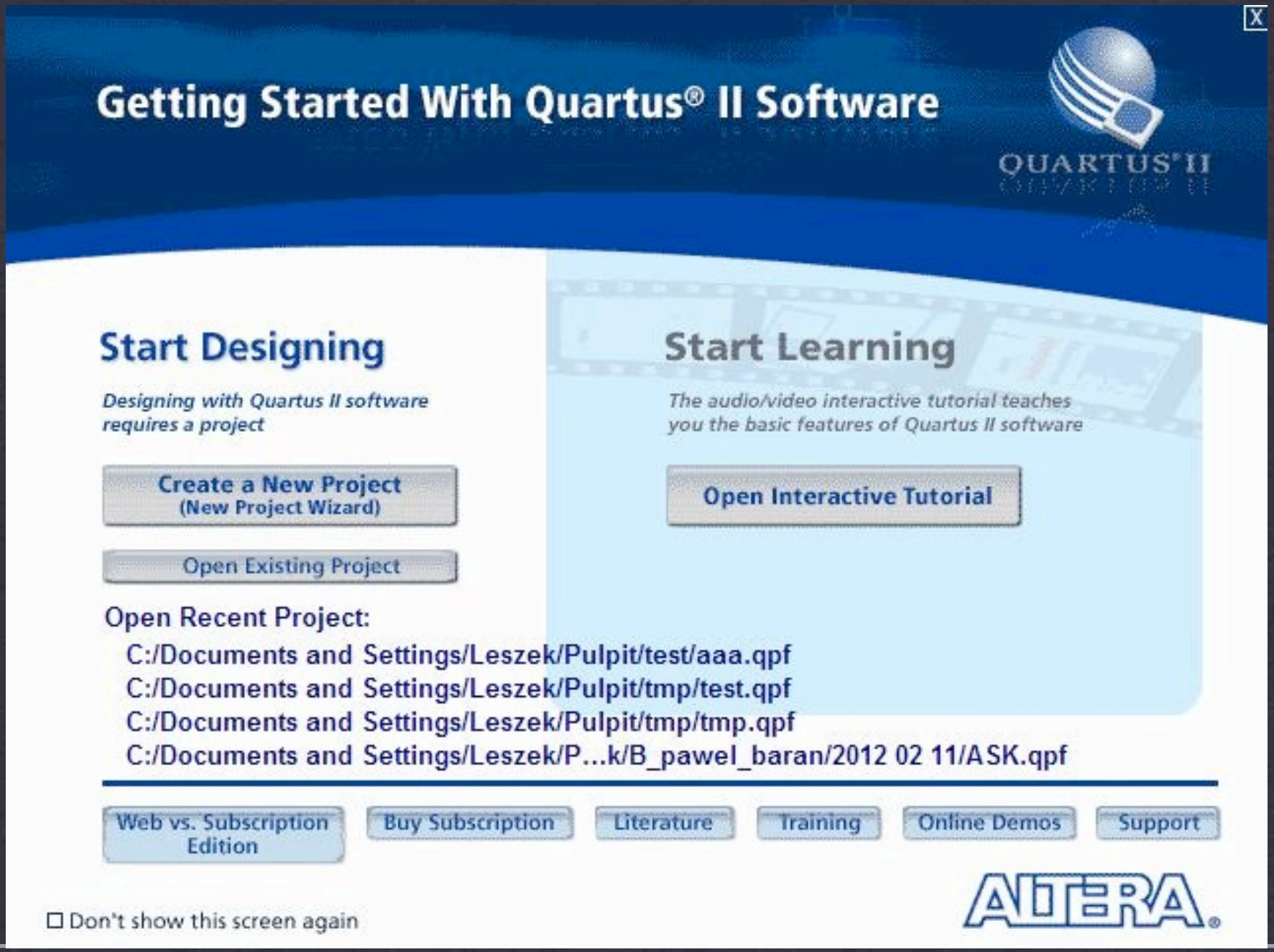
Projektowanie Systemów Wbudowanych

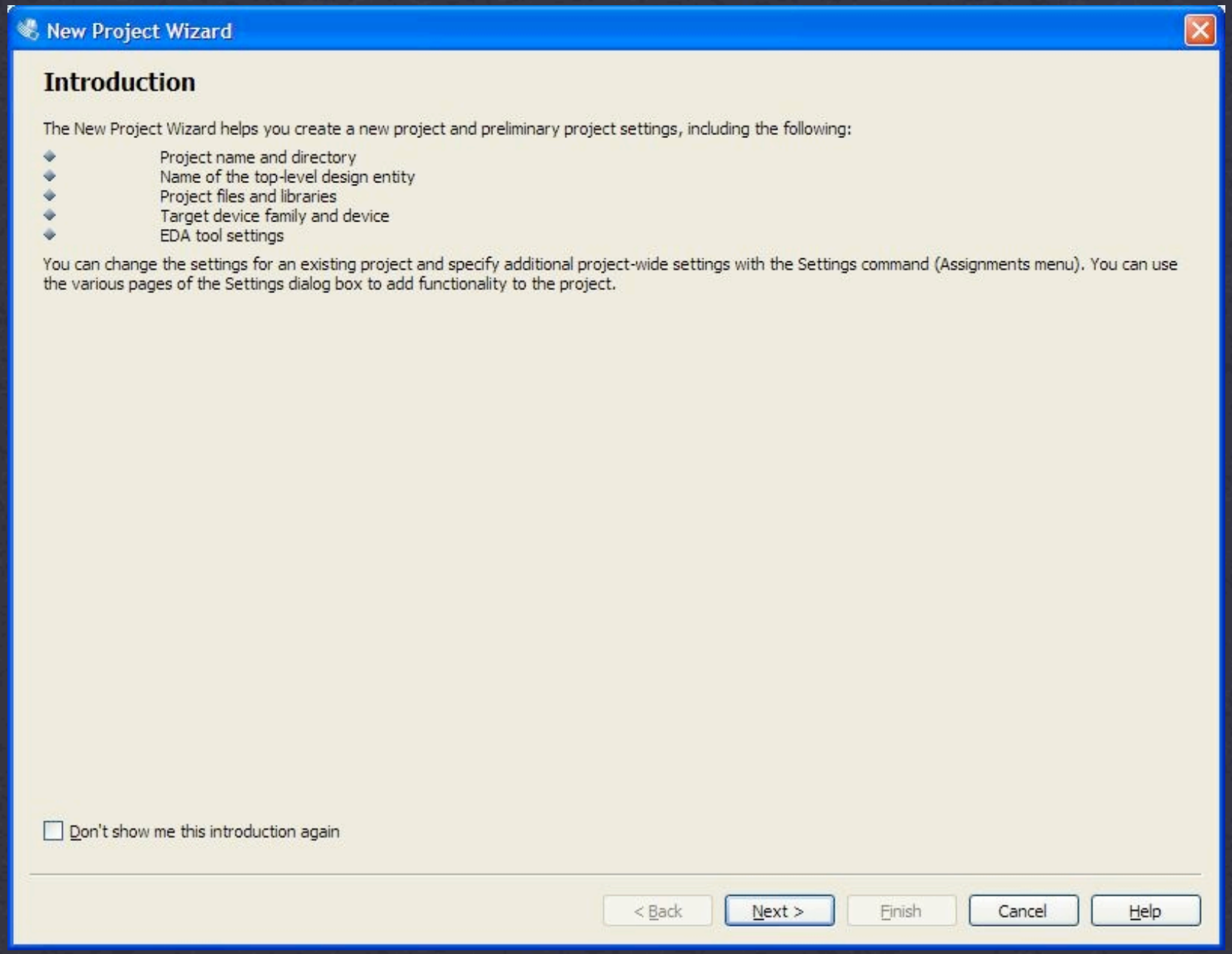
mgr inż. Leszek Ciopiński

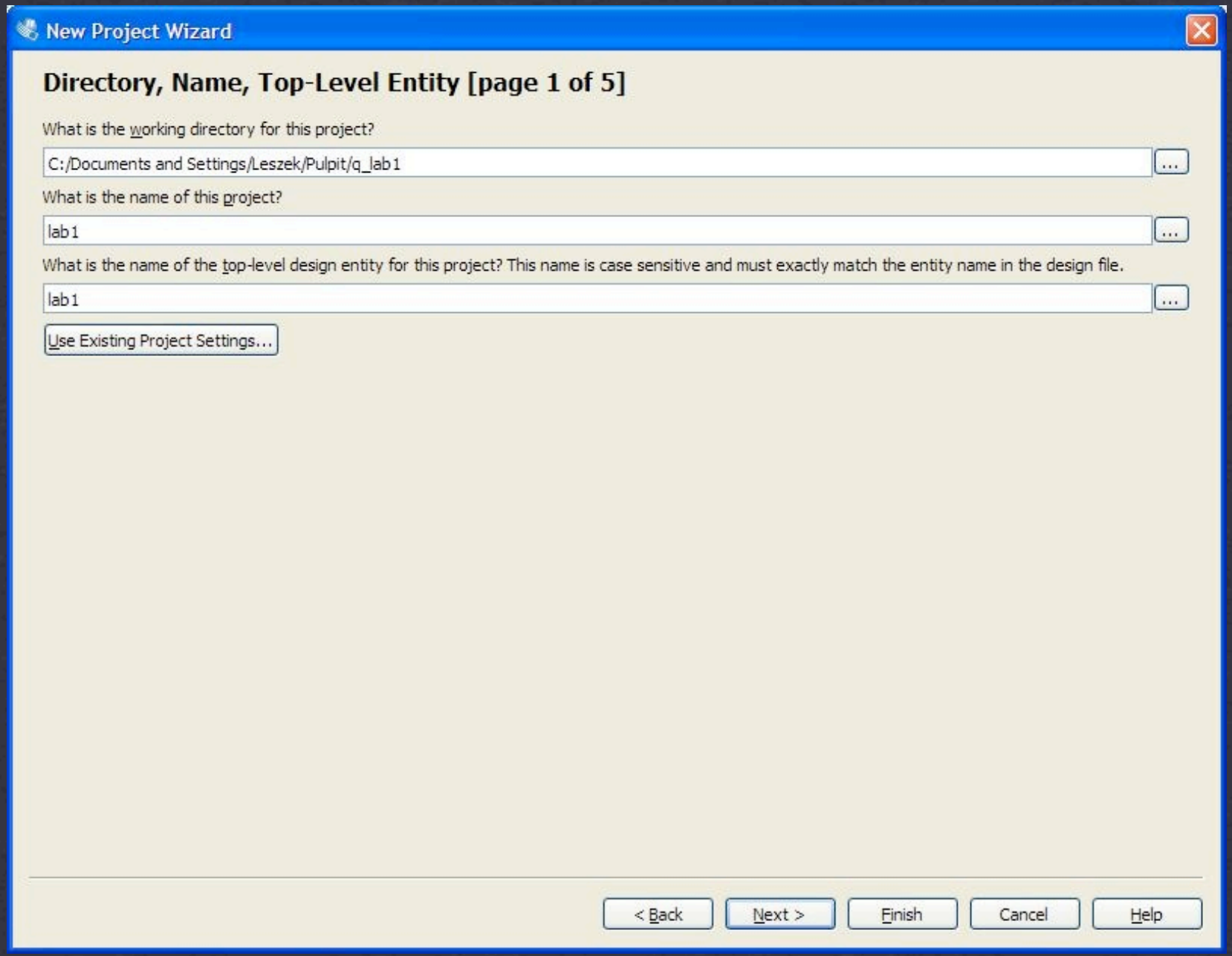
Laboratorium 1.: Szybki start.

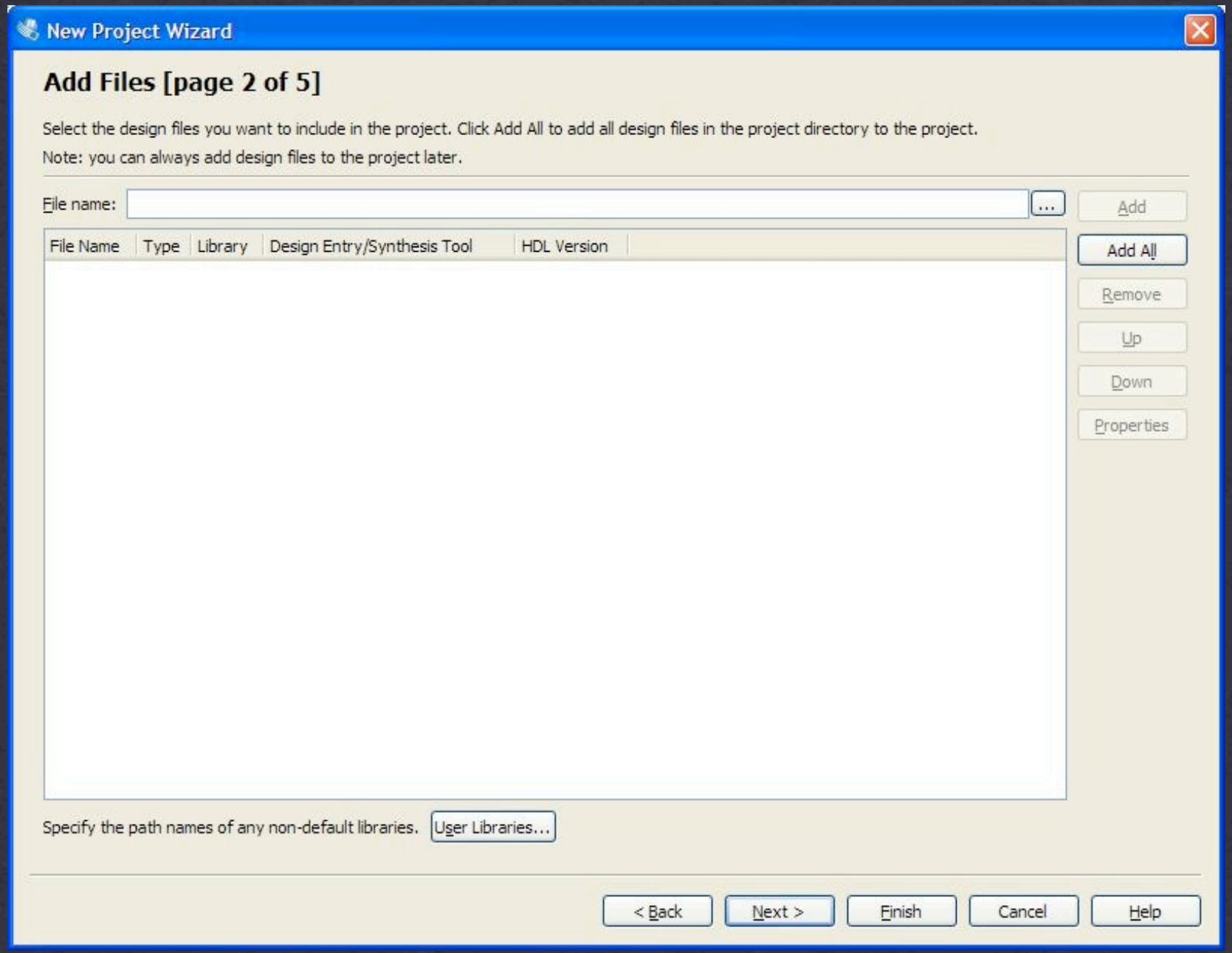


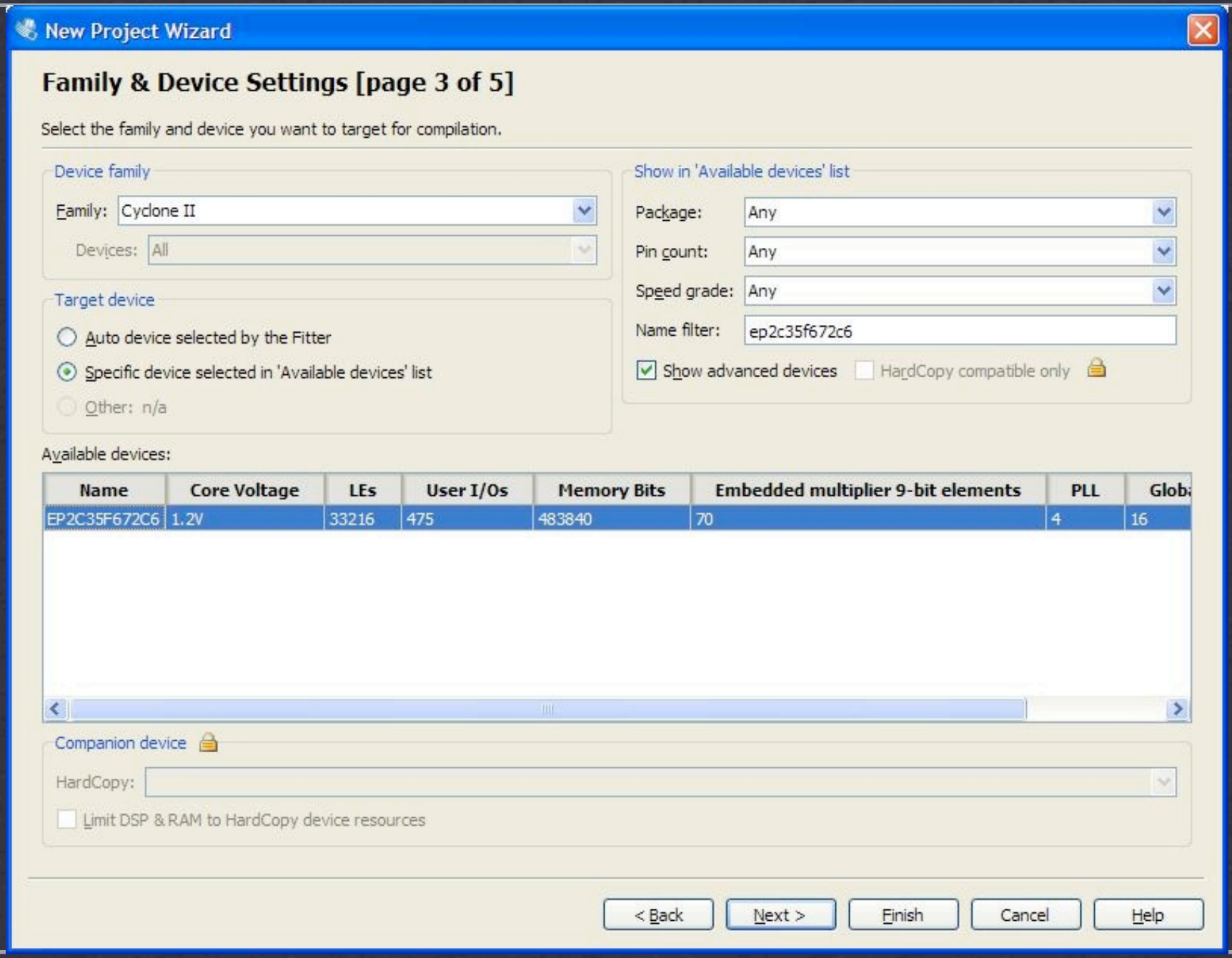
URUCHOMIĆ ŚRODOWISKO QUARTUS II

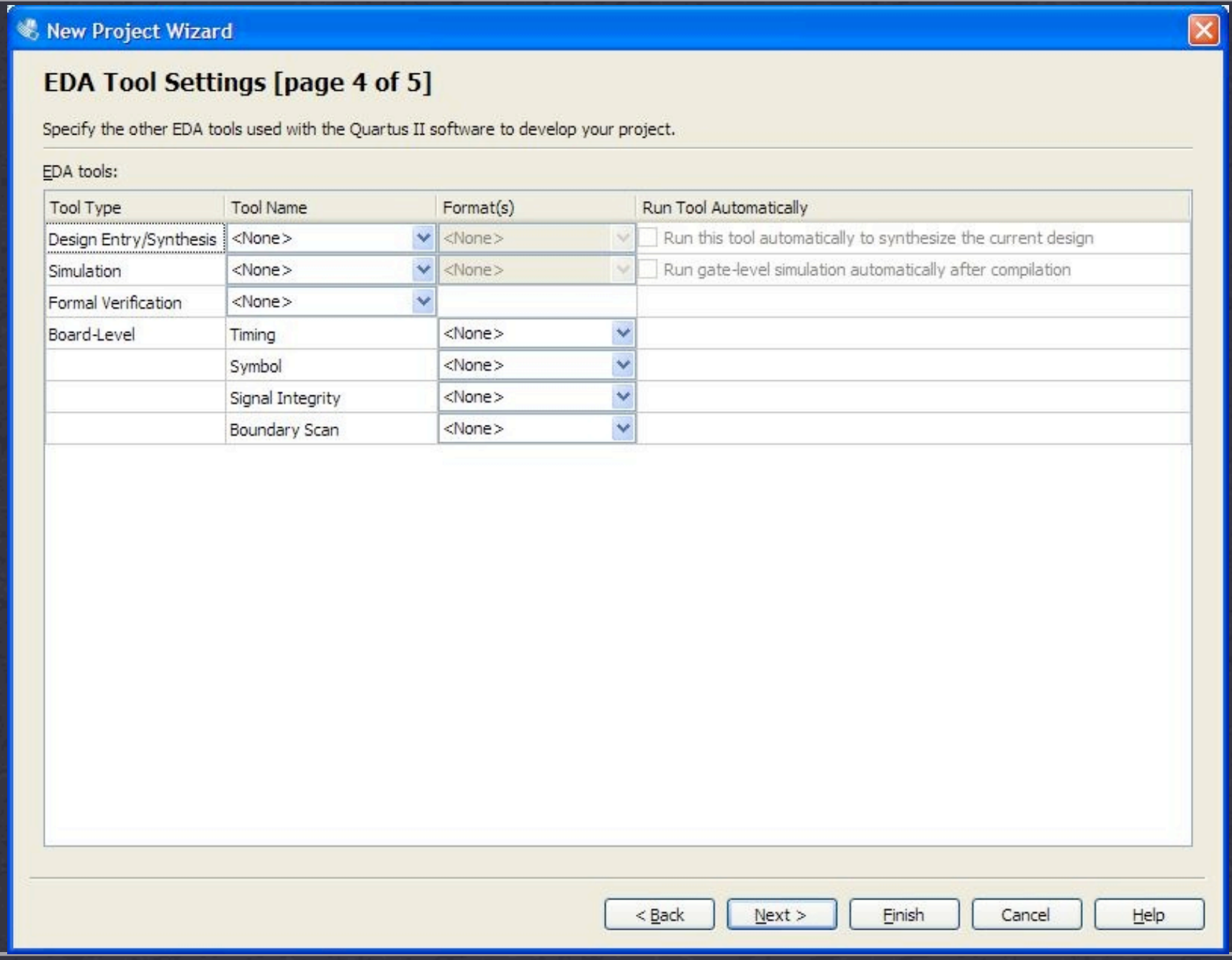
WYBRAĆ „CREATE A NEW PROJECT”

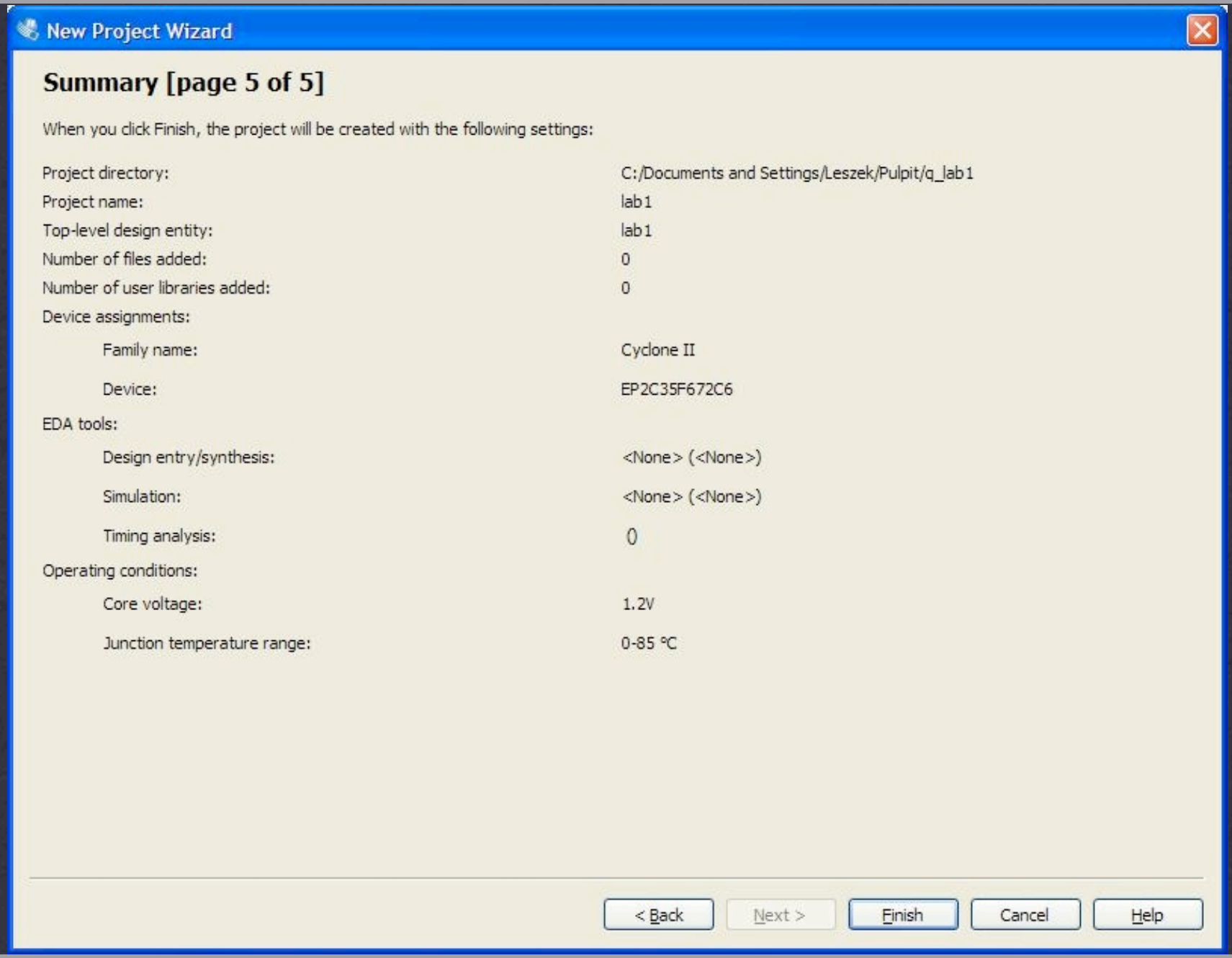

New Project Wizard
Introduction
The New Project Wizard helps you create a new project and preliminary project settings, including the following:
Project name and directory
Name of the top-level design entity
Project files and libraries
Target device family and device
EDA tool settings
You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.
Don't show me this introduction again
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Directory, Name, Top-Level Entity [page 1 of 5]
What is the working directory for this project?
C:/Documents and Settings/Leszek/Pulpit/q_lab1
...
What is the name of this project?
lab1
...
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
lab1
...
Use Existing Project Settings...
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Add Files [page 2 of 5]
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
Note: you can always add design files to the project later.
File name:
...
Add
Add All
Remove
Up
Down
Properties
File Name
Type
Library
Design Entry/Synthesis Tool
HDL Version
Specify the path names of any non-default libraries.
User Libraries...
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Family & Device Settings [page 3 of 5]
Select the family and device you want to target for compilation.
Device family
Family: Cyclone II
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Name filter: ep2c35f672c6
Show advanced devices
HardCopy compatible only
Available devices:
Name
Core Voltage
LEs
User I/Os
Memory Bits
Embedded multiplier 9-bit elements
PLL
Glob
EP2C35F672C6
1.2V
33216
475
483840
70
4
16
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
< Back
Next >
Finish
Cancel
Help


New Project Wizard
EDA Tool Settings [page 4 of 5]
Specify the other EDA tools used with the Quartus II software to develop your project.
EDA tools:
Tool Type
Tool Name
Format(s)
Run Tool Automatically
Design Entry/Synthesis
<None>
<None>
Run this tool automatically to synthesize the current design
Simulation
<None>
<None>
Run gate-level simulation automatically after compilation
Formal Verification
<None>
Board-Level
Timing
<None>
Symbol
<None>
Signal Integrity
<None>
Boundary Scan
<None>
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory: C:/Documents and Settings/Leszek/Pulpit/q_lab1
Project name: lab1
Top-level design entity: lab1
Number of files added: 0
Number of user libraries added: 0
Device assignments:
Family name: Cyclone II
Device: EP2C35F672C6
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: <None> (<None>)
Timing analysis: 0
Operating conditions:
Core voltage: 1.2V
Junction temperature range: 0-85 °C
< Back
Next >
Finish
Cancel
Help

Następnie wywołujemy

- File | New ... => Block Diagram / Shematic File
- File | Save As ... => nazwa projektu
- Assigments | Pin Planner
- Assigments | Import Assigments => wybrać plik „DE2_piny.qsf”
- Otworzyć Pin Planner

Pin Planner - C:/Documents and Settings/Leszek/Pulpit/q_lab1/lab1 - lab1

File Edit View Processing Tools Window Help

Search altera.com

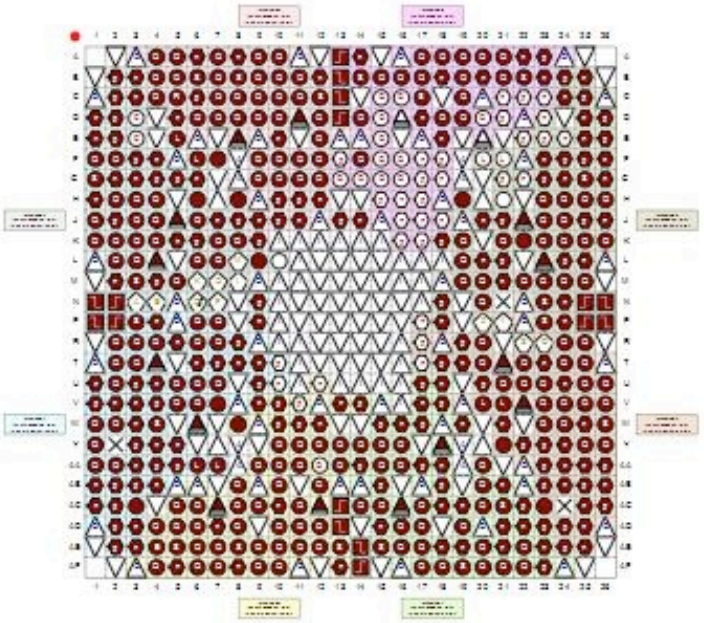
Report

Report not available

Tasks

Run Ana
Early Pin
Early
Run
Expo
Change
Show

Top View - Wire Bond
Cyclone II - EP2C35F672C6

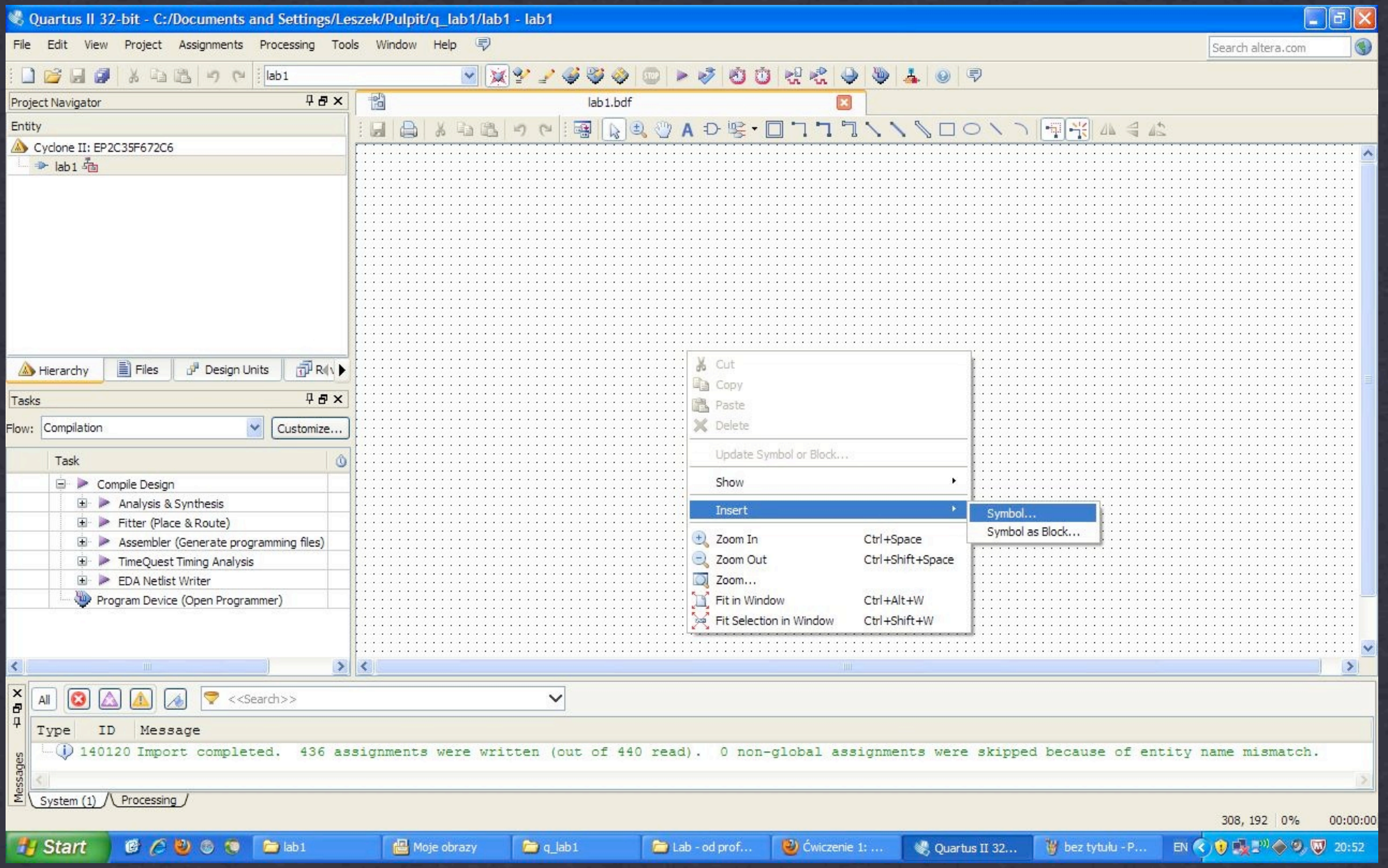


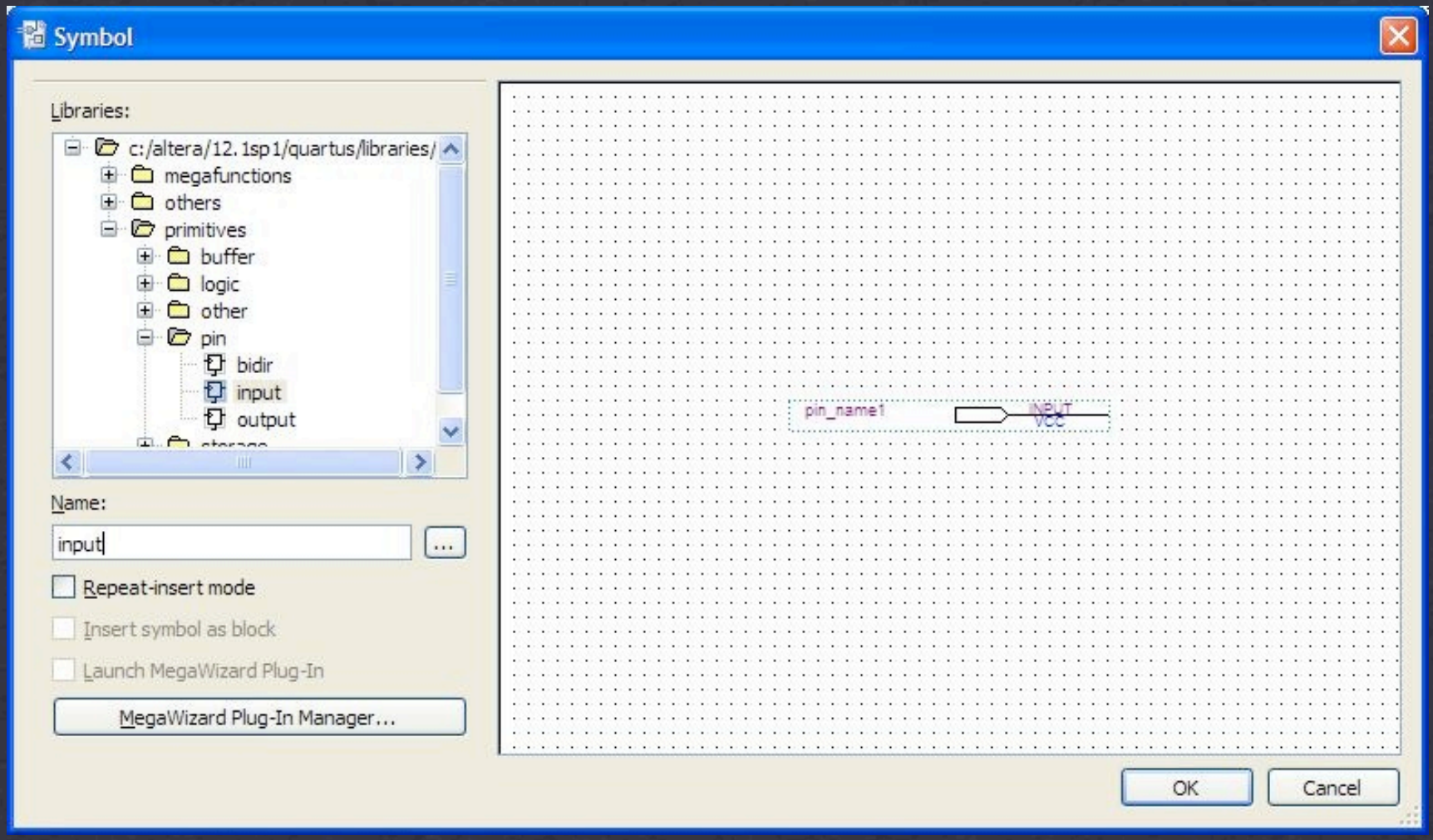
Named: * Edit: Filter: Pins: all

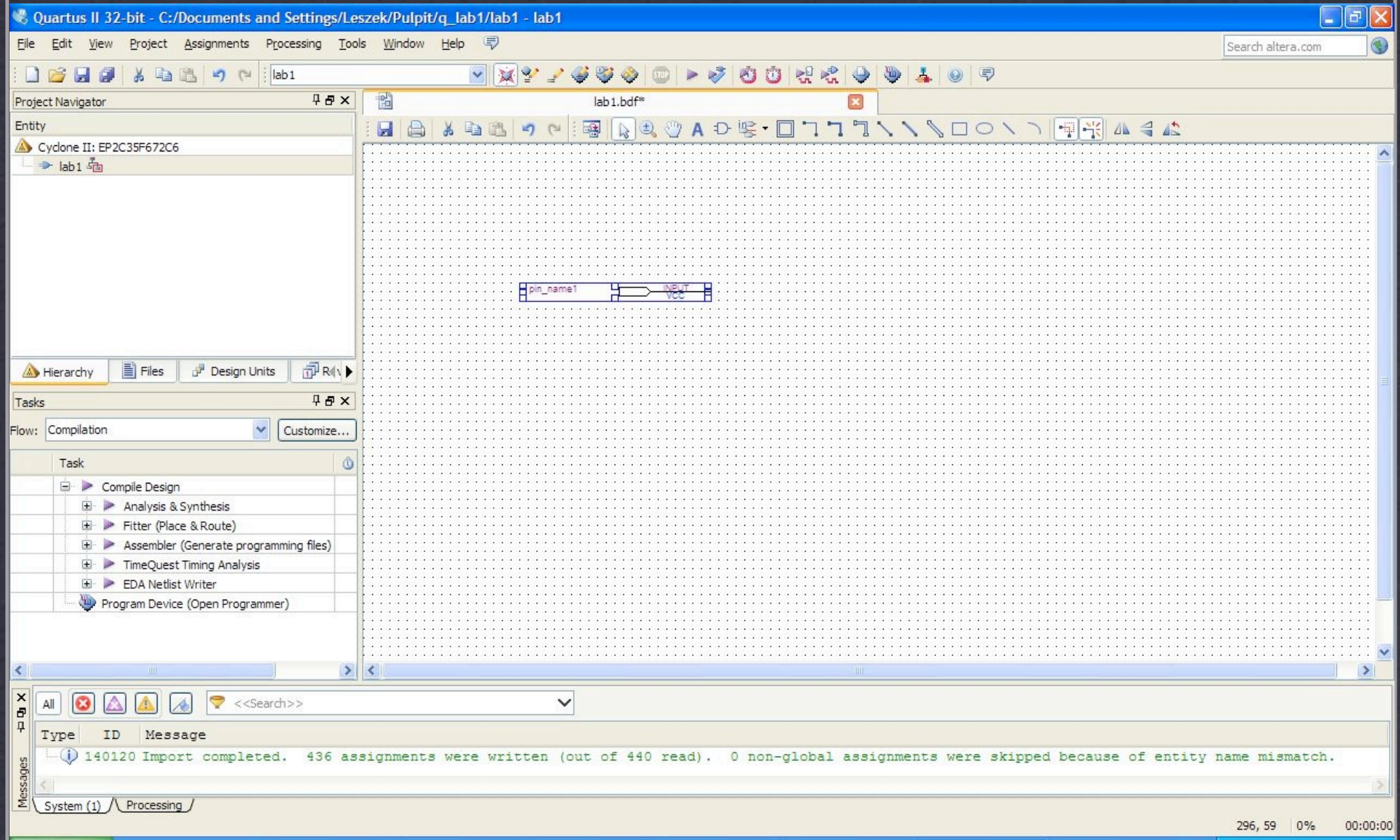
Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
SW[0]	Unknown	PIN_N25	5	B5_N1	3.3-V LV...default)	
SW[1]	Unknown	PIN_N26	5	B5_N1	3.3-V LV...default)	
SW[2]	Unknown	PIN_P25	6	B6_N0	3.3-V LV...default)	
SW[3]	Unknown	PIN_AE14	7	B7_N1	3.3-V LV...default)	
SW[4]	Unknown	PIN_AF14	7	B7_N1	3.3-V LV...default)	
SW[5]	Unknown	PIN_AD13	8	B8_N0	3.3-V LV...default)	
SW[6]	Unknown	PIN_AC13	8	B8_N0	3.3-V LV...default)	
SW[7]	Unknown	PIN_C13	3	B3_N0	3.3-V LV...default)	
SW[8]	Unknown	PIN_B13	4	B4_N1	3.3-V LV...default)	

All Pins

0% 00:00:00


Quartus II 32-bit - C:/Documents and Settings/Leszek/Pulpit/q_lab1/lab1 - lab1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
lab1
Project Navigator
Entity
Cyclone II: EP2C35F672C6
lab1
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
lab1.bdf
Cut
Copy
Paste
Delete
Update Symbol or Block...
Show
Insert
Symbol...
Symbol as Block...
Zoom In Ctrl+Space
Zoom Out Ctrl+Shift+Space
Zoom...
Fit in Window Ctrl+Alt+W
Fit Selection in Window Ctrl+Shift+W
All
<<Search>>
Type ID Message
140120 Import completed. 436 assignments were written (out of 440 read). 0 non-global assignments were skipped because of entity name mismatch.
Messages
System (1) Processing
308, 192 0% 00:00:00
Start
lab1
Moje obrazy
q_lab1
Lab - od prof...
Ćwiczenie 1: ...
Quartus II 32...
bez tytułu - P...
EN
20:52


Symbol
Libraries:
c:/altera/12.1sp1/quartus/libraries/
megafunctions
others
primitives
buffer
logic
other
pin
bidir
input
output
Name:
input
...
Repeat-insert mode
Insert symbol as block
Launch MegaWizard Plug-In
MegaWizard Plug-In Manager...
pin_name1
INPUT
VCC
OK
Cancel


Quartus II 32-bit - C:/Documents and Settings/Leszek/Pulpit/q_lab1/lab1 - lab1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
lab1
Project Navigator
Entity
Cyclone II: EP2C35F672C6
lab1
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
lab1.bdf*
pin_name1
INPUT
VCC
All
<<Search>>
Type ID Message
140120 Import completed. 436 assignments were written (out of 440 read). 0 non-global assignments were skipped because of entity name mismatch.
Messages
System (1) Processing
296, 59 0% 00:00:00

Do wykonania

- Kliknąć 2 razy i zmienić nazwę na SW[2..0]
- dodać elementy:
  - output
  - and2
  - or2
- Skopiować wejścia i połączyć

Quartus II 32-bit - C:/Documents and Settings/Leszek/Pulpit/q_lab1/lab1 - lab1

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

lab1

Project Navigator

Entity

Cyclone II: EP2C35F672C6

lab1

Hierarchy Files Design Units

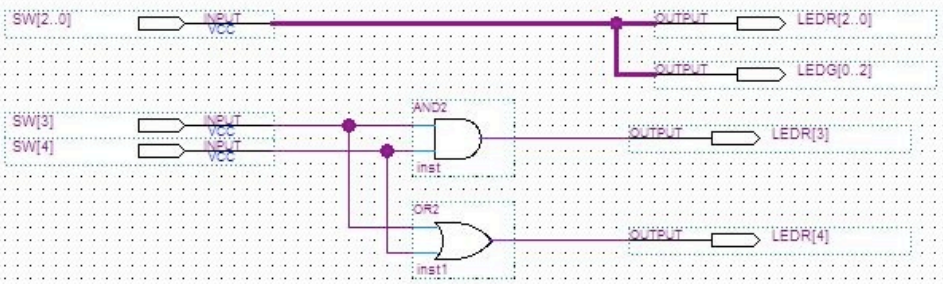
Tasks

Flow: Compilation Customize...

Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming files)
  - TimeQuest Timing Analysis
  - EDA Netlist Writer
  - Program Device (Open Programmer)

lab1.bdf



All <<Search>>

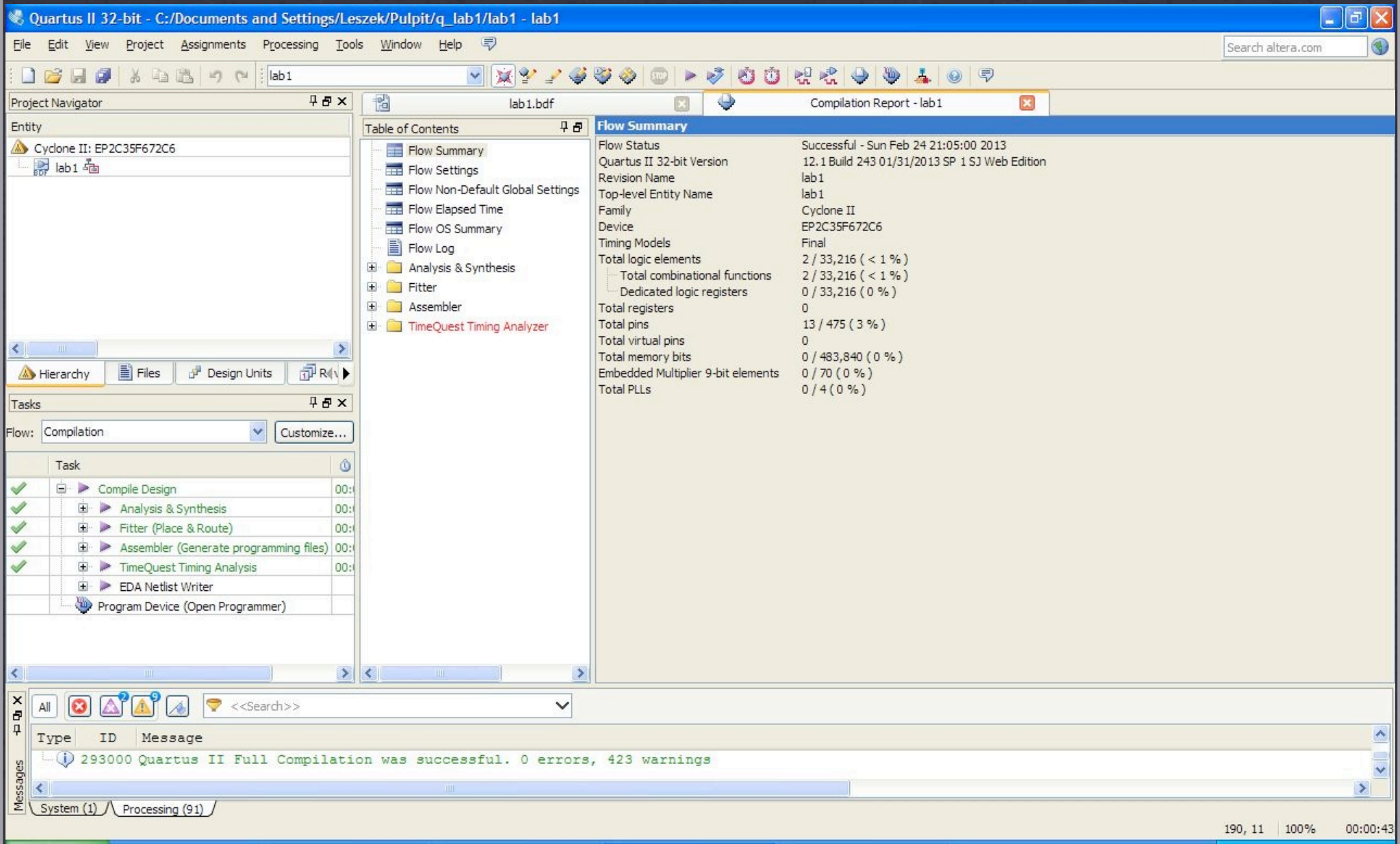
Type	ID	Message
	140120	Import completed. 436 assignments were written (out of 440 read). 0 non-global assignments were skipped because of entity name mismatch.

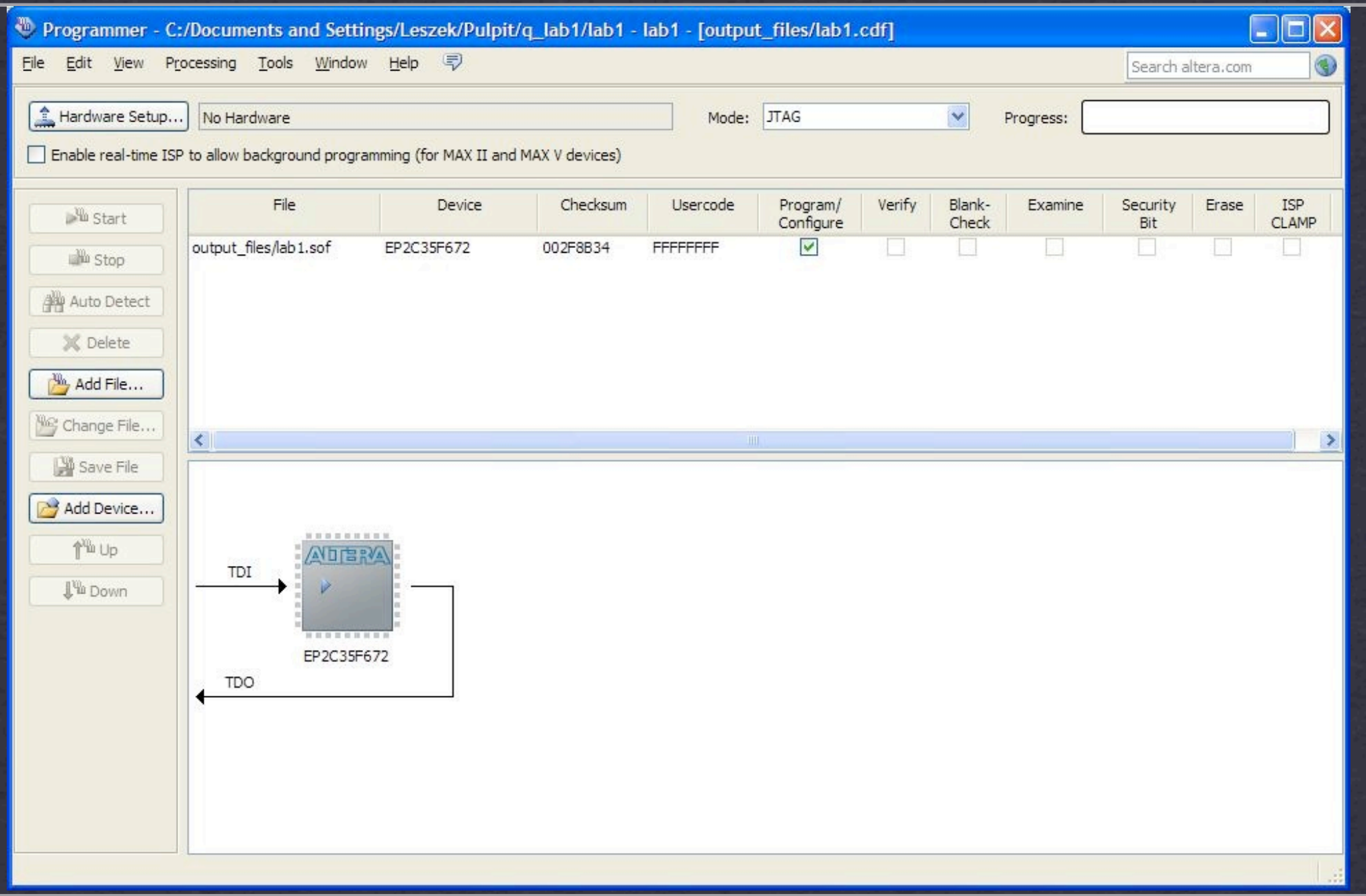
Messages

System (1) Processing

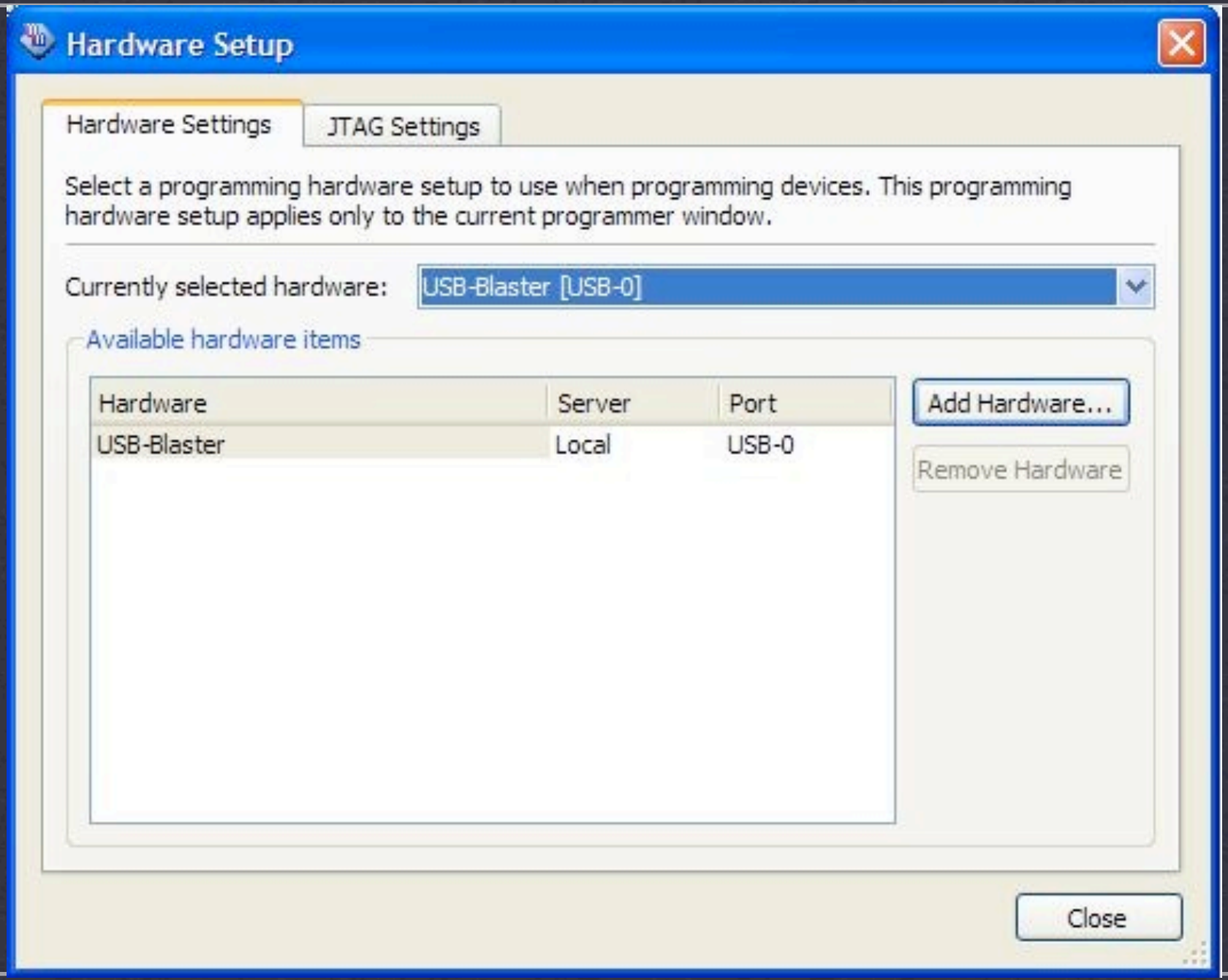
Reverses the last action

190, 11 0% 00:00:00


Quartus II 32-bit - C:/Documents and Settings/Leszek/Pulpit/q_lab1/lab1 - lab1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
lab1
Project Navigator
Entity
Cyclone II: EP2C35F672C6
lab1
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)
lab1.bdf
Compilation Report - lab1
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
TimeQuest Timing Analyzer
Flow Summary
Flow Status Successful - Sun Feb 24 21:05:00 2013
Quartus II 32-bit Version 12.1 Build 243 01/31/2013 SP 1 SJ Web Edition
Revision Name lab1
Top-level Entity Name lab1
Family Cyclone II
Device EP2C35F672C6
Timing Models Final
Total logic elements 2 / 33,216 (< 1 %)
Total combinational functions 2 / 33,216 (< 1 %)
Dedicated logic registers 0 / 33,216 (0 %)
Total registers 0
Total pins 13 / 475 (3 %)
Total virtual pins 0
Total memory bits 0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements 0 / 70 (0 %)
Total PLLs 0 / 4 (0 %)
All
<<Search>>
Type ID Message
293000 Quartus II Full Compilation was successful. 0 errors, 423 warnings
Messages
System (1) Processing (91)
190, 11 100% 00:00:43

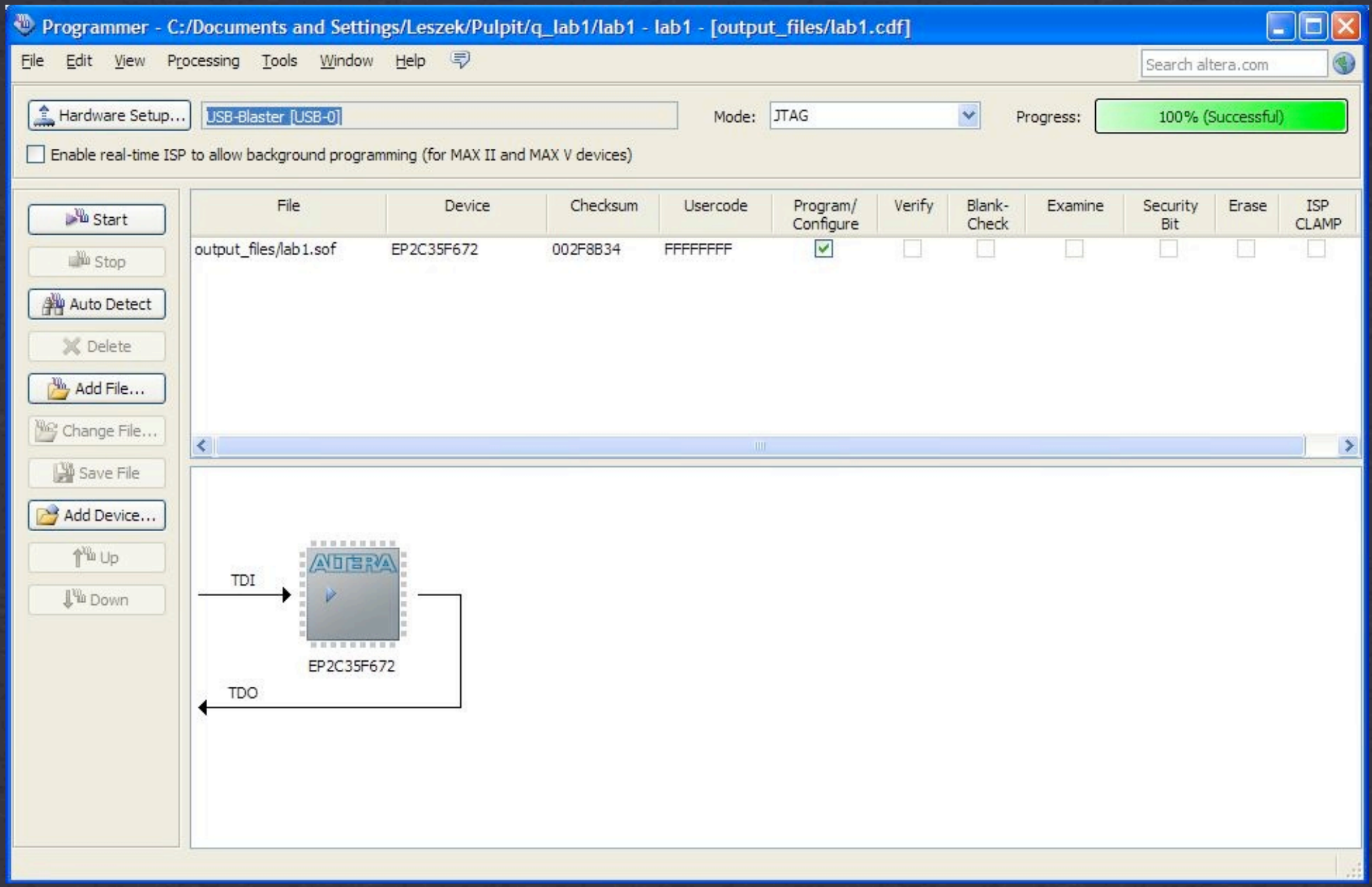


WYBRAĆ TOOL I PROGRAMMER



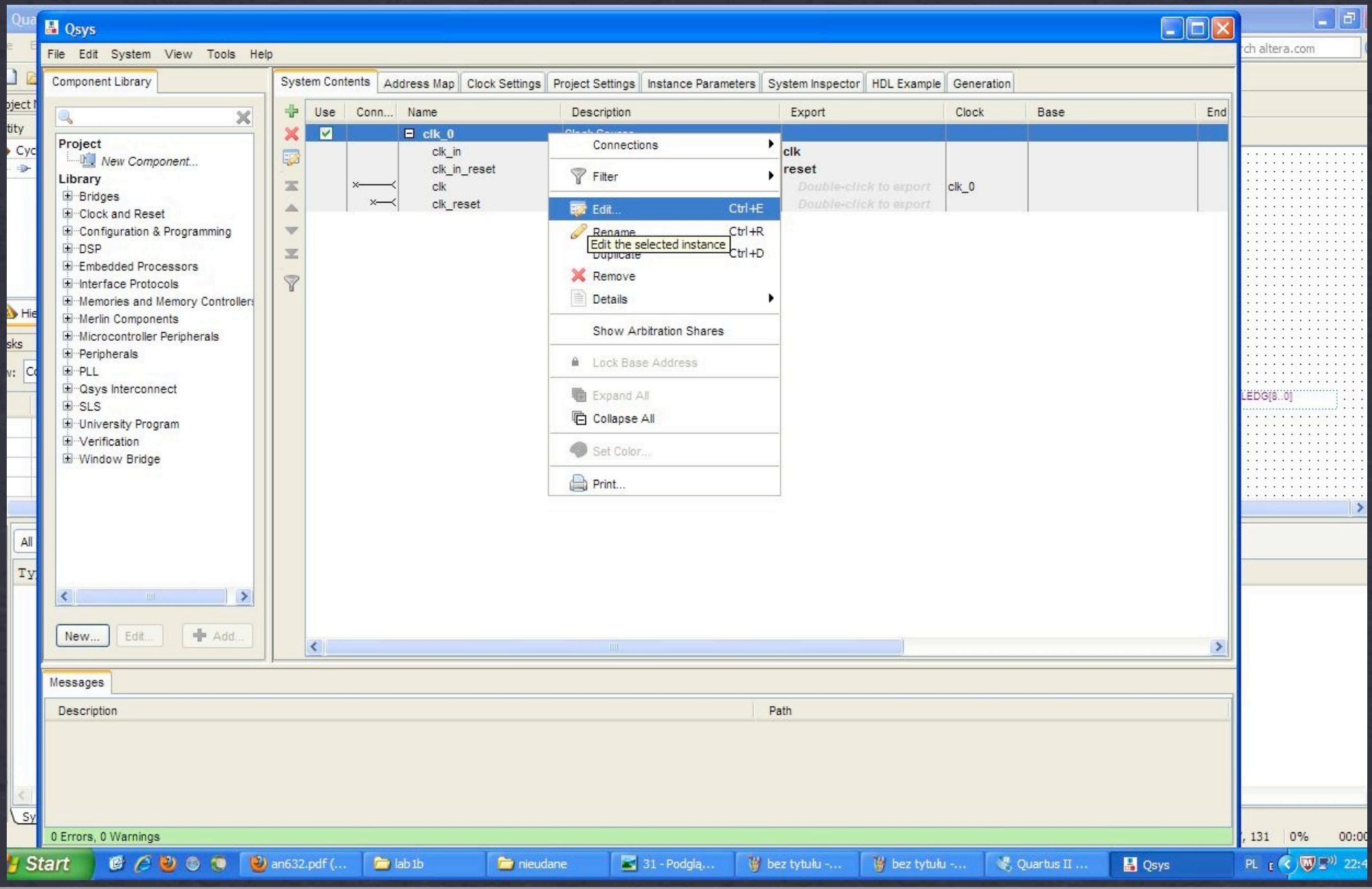
WYBRAĆ HARDWARE SETUP

I WYBRAĆ USB BLASTER



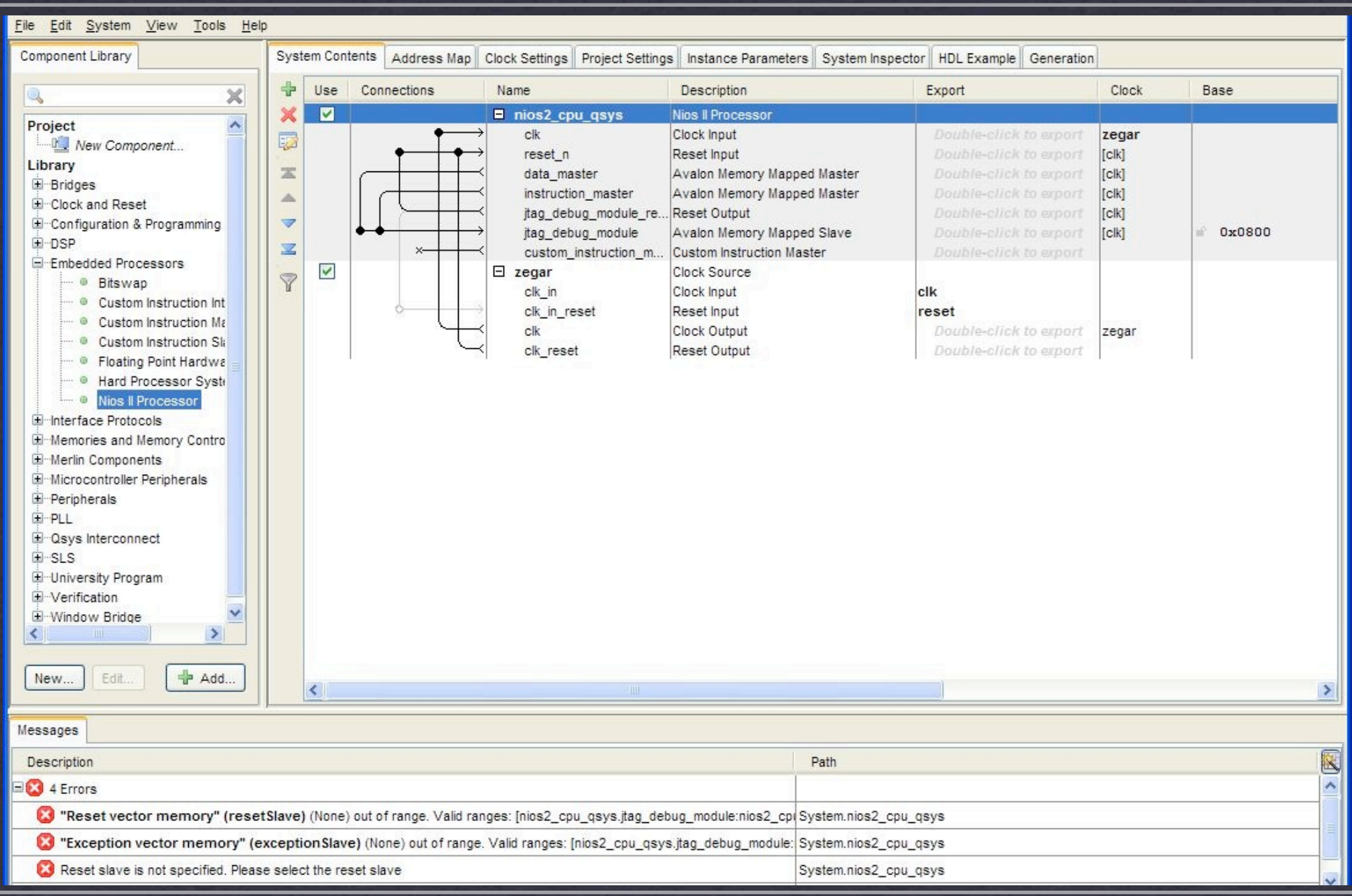
WYBRAĆ START

Qsys



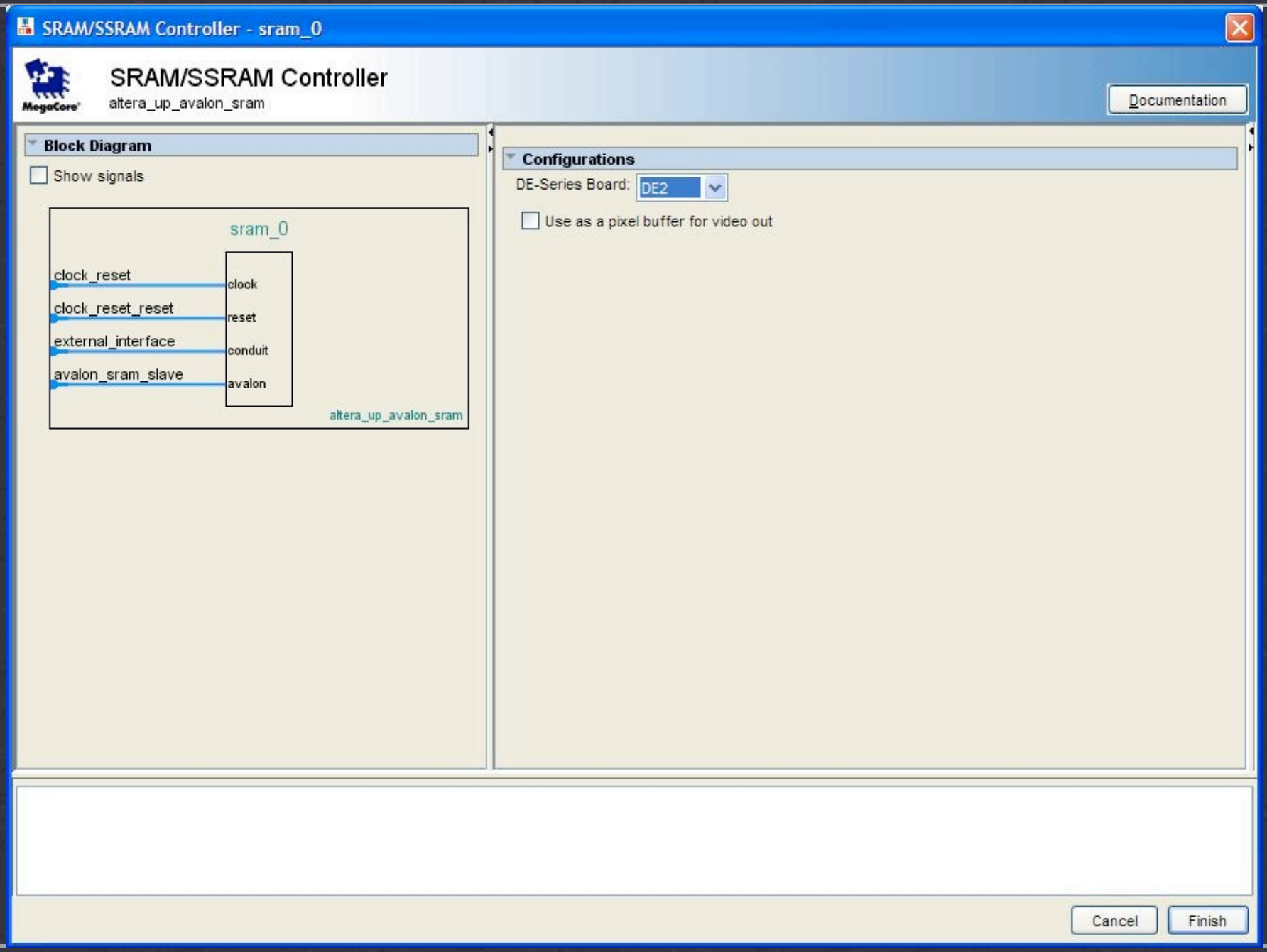
FILE | NEW ... QSYS SYSTEM FILE

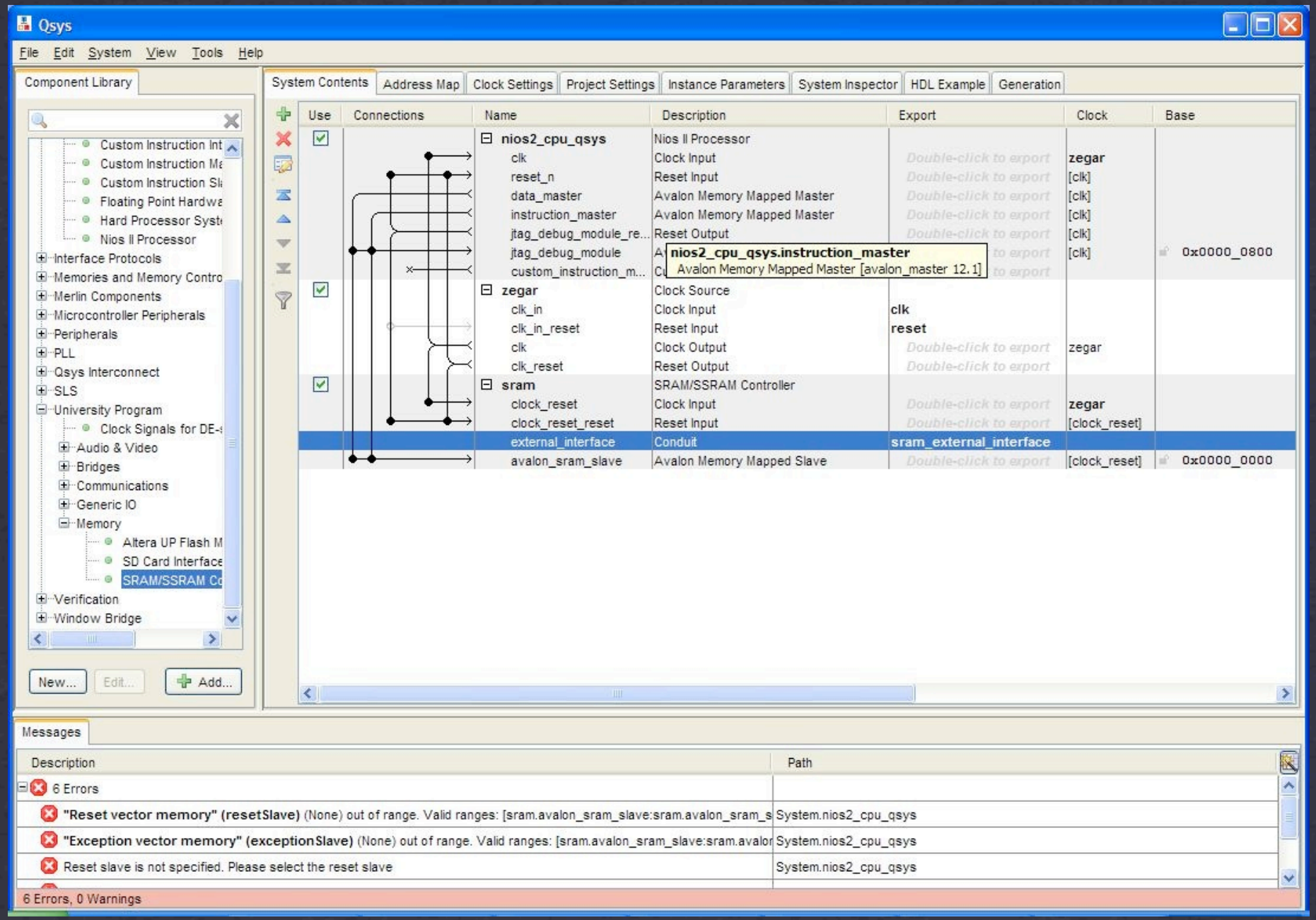
ZMIANA NAZWY ZEGARA -> RENAME

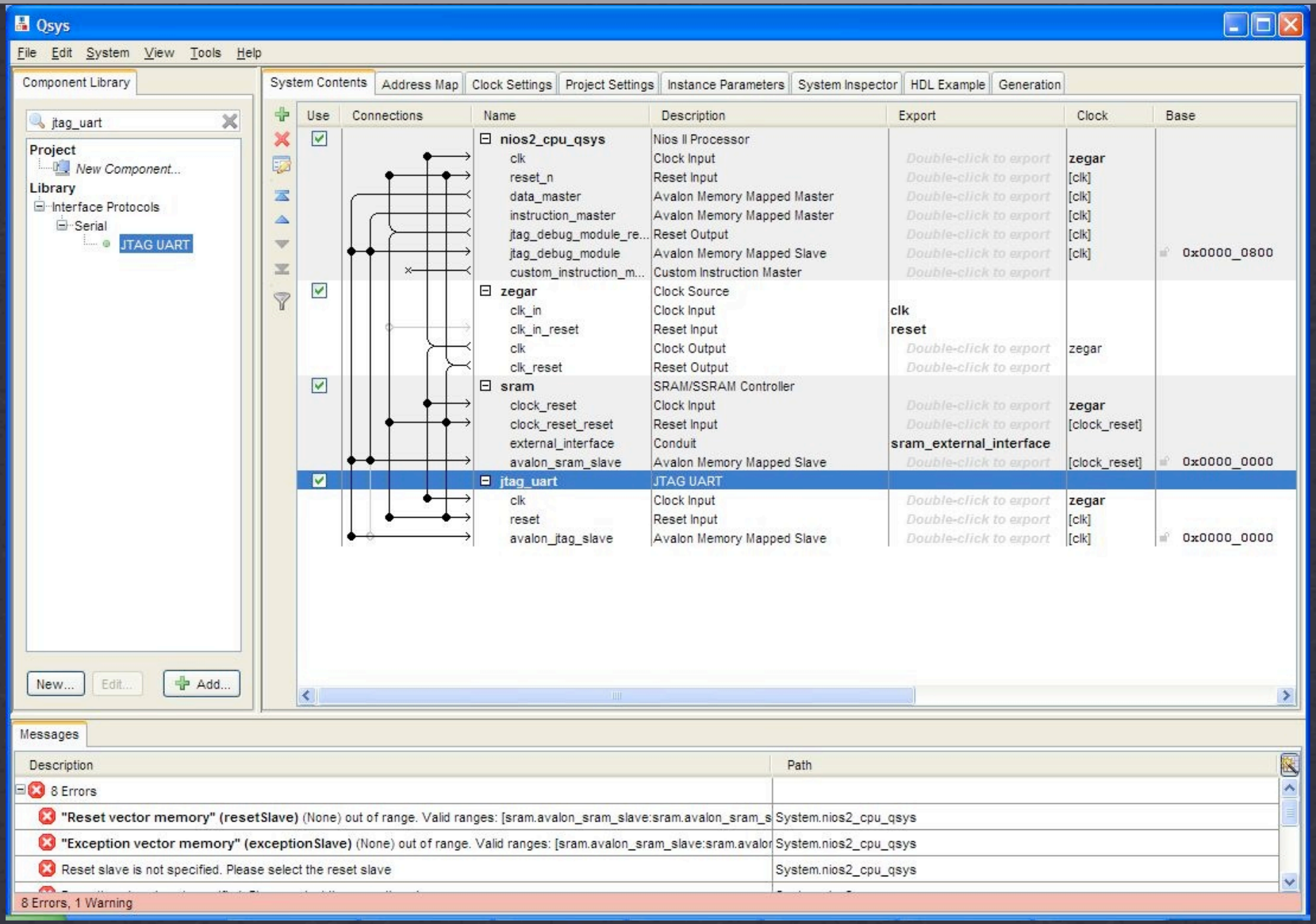


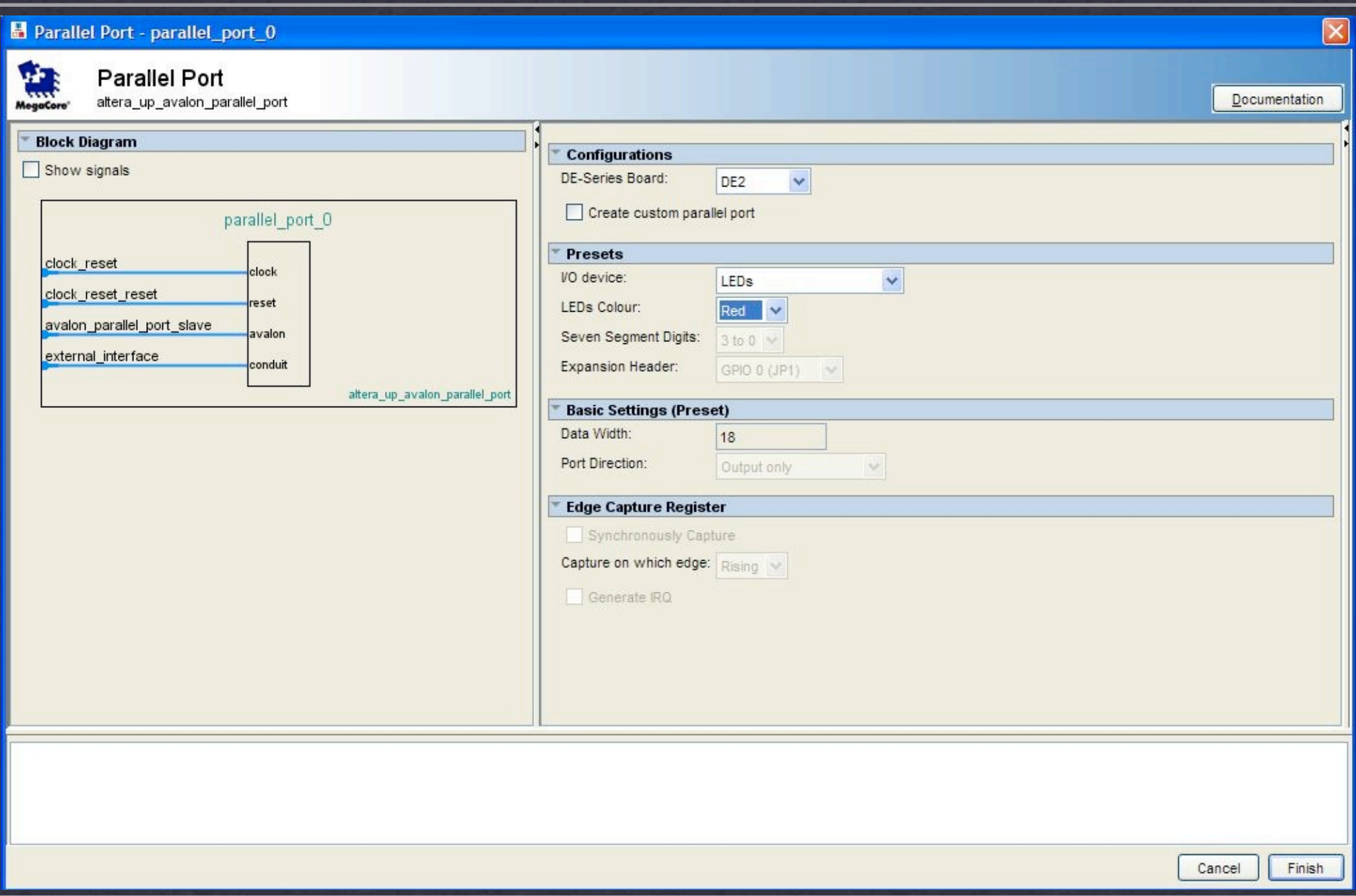
DODAJEMY PROCESOR

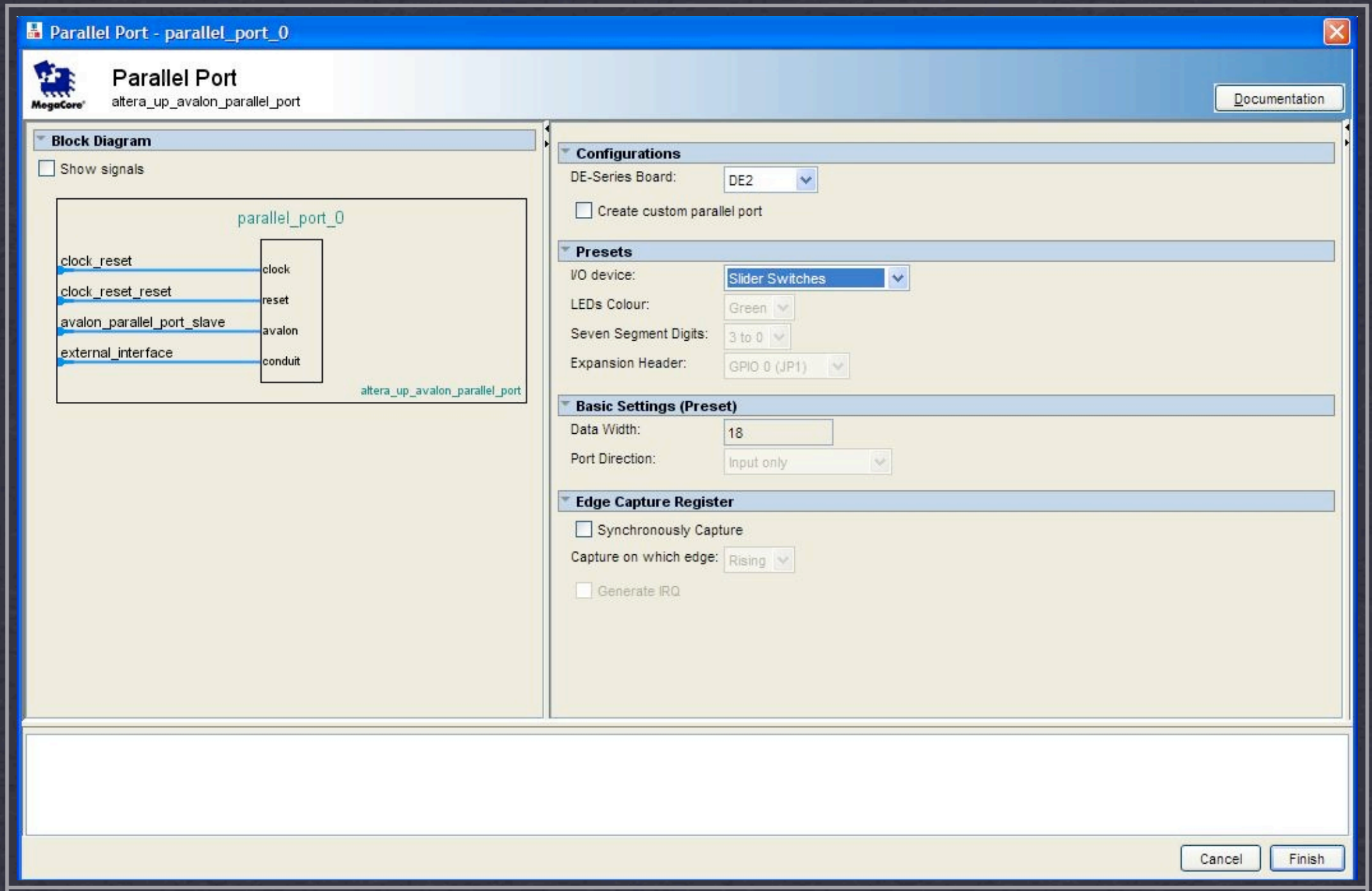
NIOS II WERSJA II/E

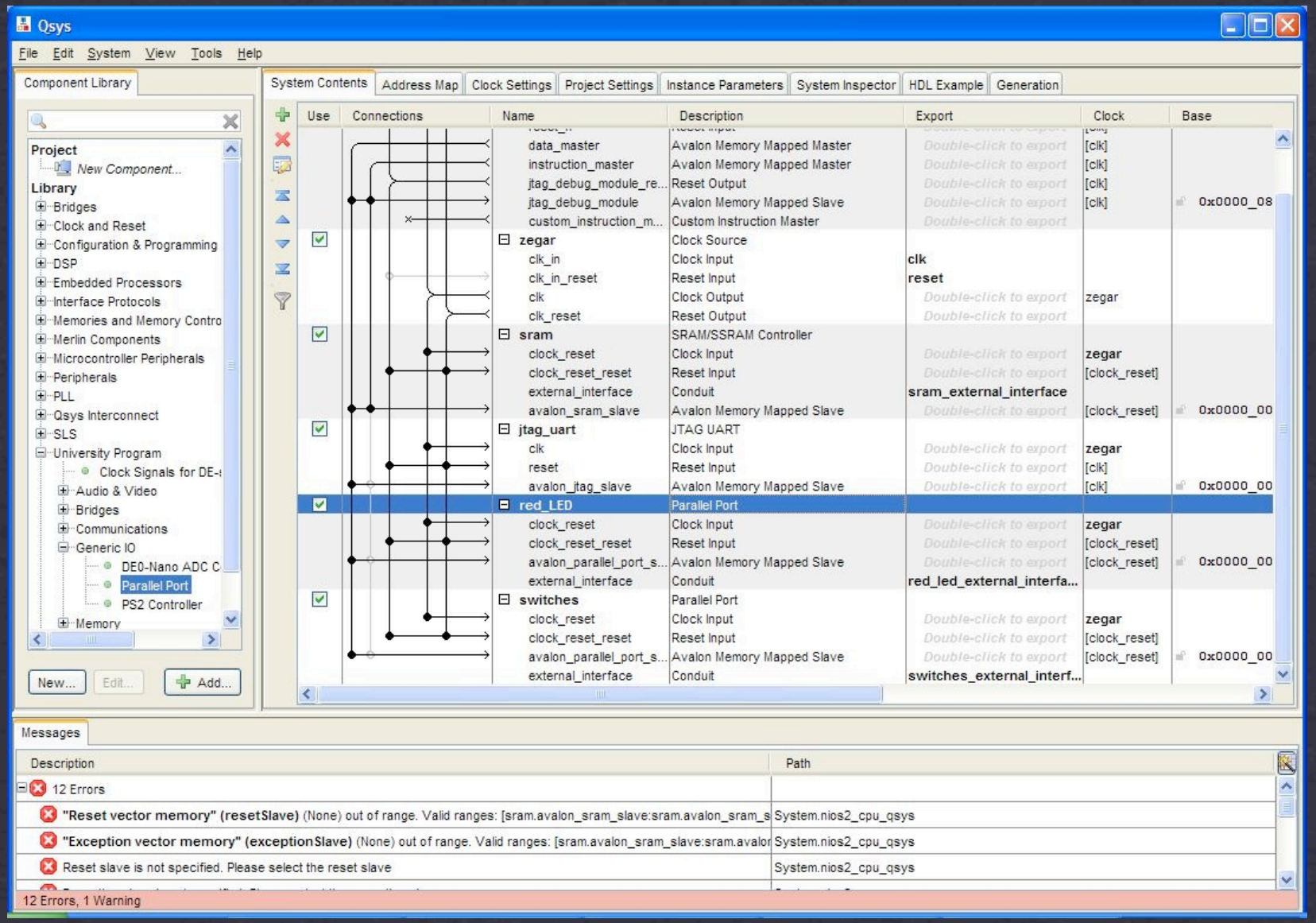

SRAM/SSRAM Controller - sram_0
SRAM/SSRAM Controller
altera_up_avalon_sram
Documentation
Block Diagram
Show signals
sram_0
clock_reset
clock_reset_reset
external_interface
avalon_sram_slave
clock
reset
conduit
avalon
altera_up_avalon_sram
Configurations
DE-Series Board:
DE2
Use as a pixel buffer for video out
Cancel
Finish

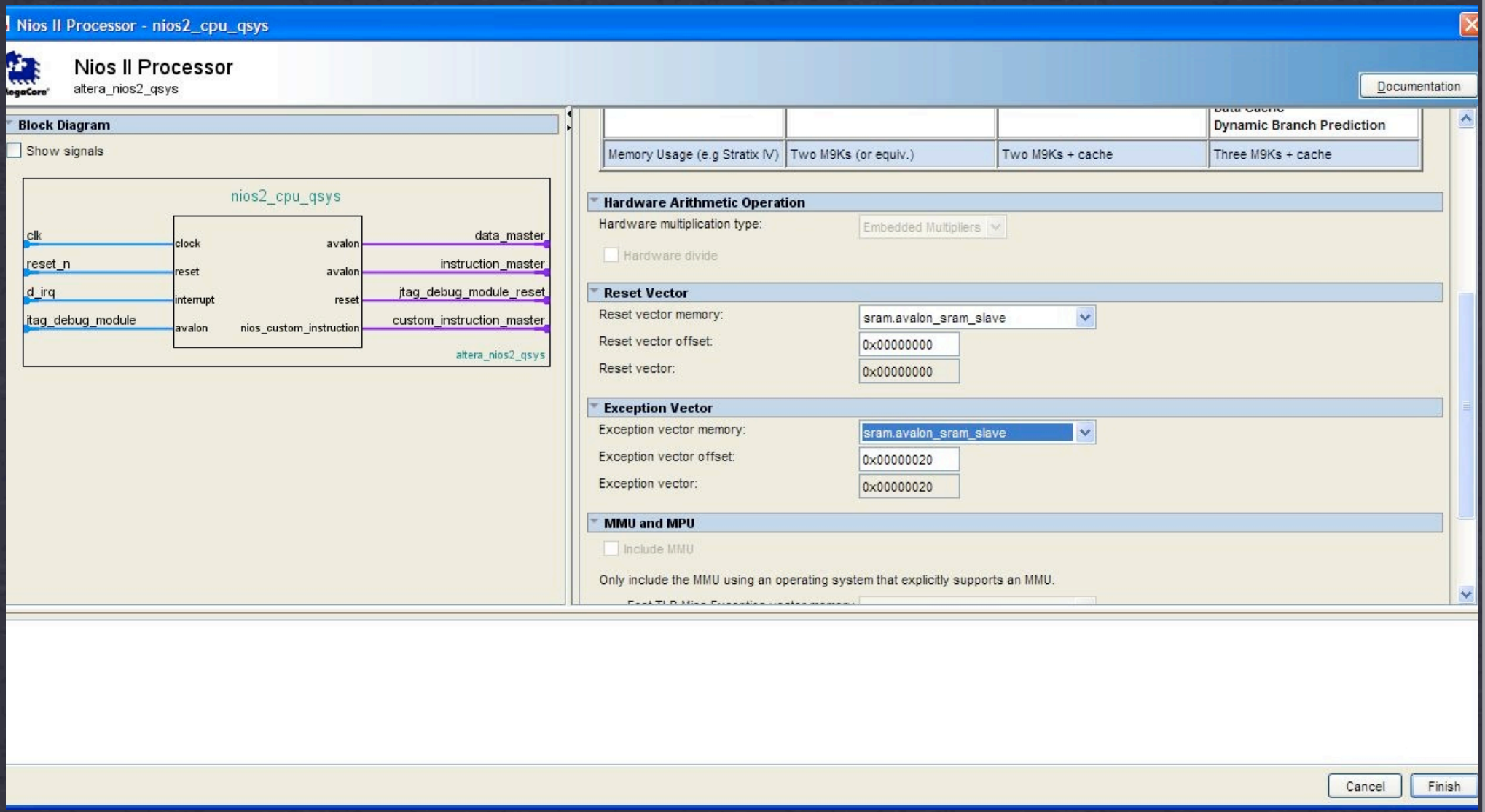

Qsys
File Edit System View Tools Help
Component Library
Custom Instruction Int
Custom Instruction Ma
Custom Instruction Sl
Floating Point Hardwa
Hard Processor Syst
Nios II Processor
Interface Protocols
Memories and Memory Contro
Merlin Components
Microcontroller Peripherals
Peripherals
PLL
Qsys Interconnect
SLS
University Program
Clock Signals for DE-
Audio & Video
Bridges
Communications
Generic IO
Memory
Altera UP Flash M
SD Card Interface
SRAM/SSRAM Co
Verification
Window Bridge
New...
Edit...
Add...
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
nios2_cpu_qsys
Nios II Processor
clk
Clock Input
zegar
reset_n
Reset Input
[clk]
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
jtag_debug_module_re...
Reset Output
jtag_debug_module
0x0000_0800
custom_instruction_m...
nios2_cpu_qsys.instruction_master
Avalon Memory Mapped Master [avalon_master 12.1]
zegar
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
zegar
clk_reset
Reset Output
sram
SRAM/SSRAM Controller
clock_reset
Clock Input
zegar
clock_reset_reset
Reset Input
[clock_reset]
external_interface
Conduit
sram_external_interface
avalon_sram_slave
Avalon Memory Mapped Slave
[clock_reset]
0x0000_0000
Double-click to export
Messages
Description
Path
6 Errors
"Reset vector memory" (resetSlave) (None) out of range. Valid ranges: [sram.avalon_sram_slave:sram.avalon_sram_s
System.nios2_cpu_qsys
"Exception vector memory" (exceptionSlave) (None) out of range. Valid ranges: [sram.avalon_sram_slave:sram.avalor
System.nios2_cpu_qsys
Reset slave is not specified. Please select the reset slave
System.nios2_cpu_qsys
6 Errors, 0 Warnings


Qsys
File Edit System View Tools Help
Component Library
jtag_uart
Project
New Component...
Library
Interface Protocols
Serial
JTAG UART
New... Edit... Add...
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
nios2_cpu_qsys
Nios II Processor
clk
Clock Input
zegar
reset_n
Reset Input
[clk]
data_master
Avalon Memory Mapped Master
[clk]
instruction_master
Avalon Memory Mapped Master
[clk]
jtag_debug_module_re...
Reset Output
[clk]
jtag_debug_module
Avalon Memory Mapped Slave
[clk]
0x0000_0800
custom_instruction_m...
Custom Instruction Master
zegar
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
zegar
clk_reset
Reset Output
sram
SRAM/SSRAM Controller
clock_reset
Clock Input
zegar
clock_reset_reset
Reset Input
[clock_reset]
external_interface
Conduit
sram_external_interface
avalon_sram_slave
Avalon Memory Mapped Slave
[clock_reset]
0x0000_0000
jtag_uart
JTAG UART
clk
Clock Input
zegar
reset
Reset Input
[clk]
avalon_jtag_slave
Avalon Memory Mapped Slave
[clk]
0x0000_0000
Messages
Description
Path
8 Errors
"Reset vector memory" (resetSlave) (None) out of range. Valid ranges: [sram.avalon_sram_slave:sram.avalon_sram_s
System.nios2_cpu_qsys
"Exception vector memory" (exceptionSlave) (None) out of range. Valid ranges: [sram.avalon_sram_slave:sram.avalor
System.nios2_cpu_qsys
Reset slave is not specified. Please select the reset slave
System.nios2_cpu_qsys
8 Errors, 1 Warning


Parallel Port - parallel_port_0
Parallel Port
altera_up_avalon_parallel_port
Documentation
Block Diagram
Show signals
parallel_port_0
clock_reset
clock_reset_reset
avalon_parallel_port_slave
external_interface
clock
reset
avalon
conduit
altera_up_avalon_parallel_port
Configurations
DE-Series Board:
DE2
Create custom parallel port
Presets
I/O device:
LEDs
LEDs Colour:
Red
Seven Segment Digits:
3 to 0
Expansion Header:
GPIO 0 (JP1)
Basic Settings (Preset)
Data Width:
18
Port Direction:
Output only
Edge Capture Register
Synchronously Capture
Capture on which edge:
Rising
Generate IRQ
Cancel
Finish

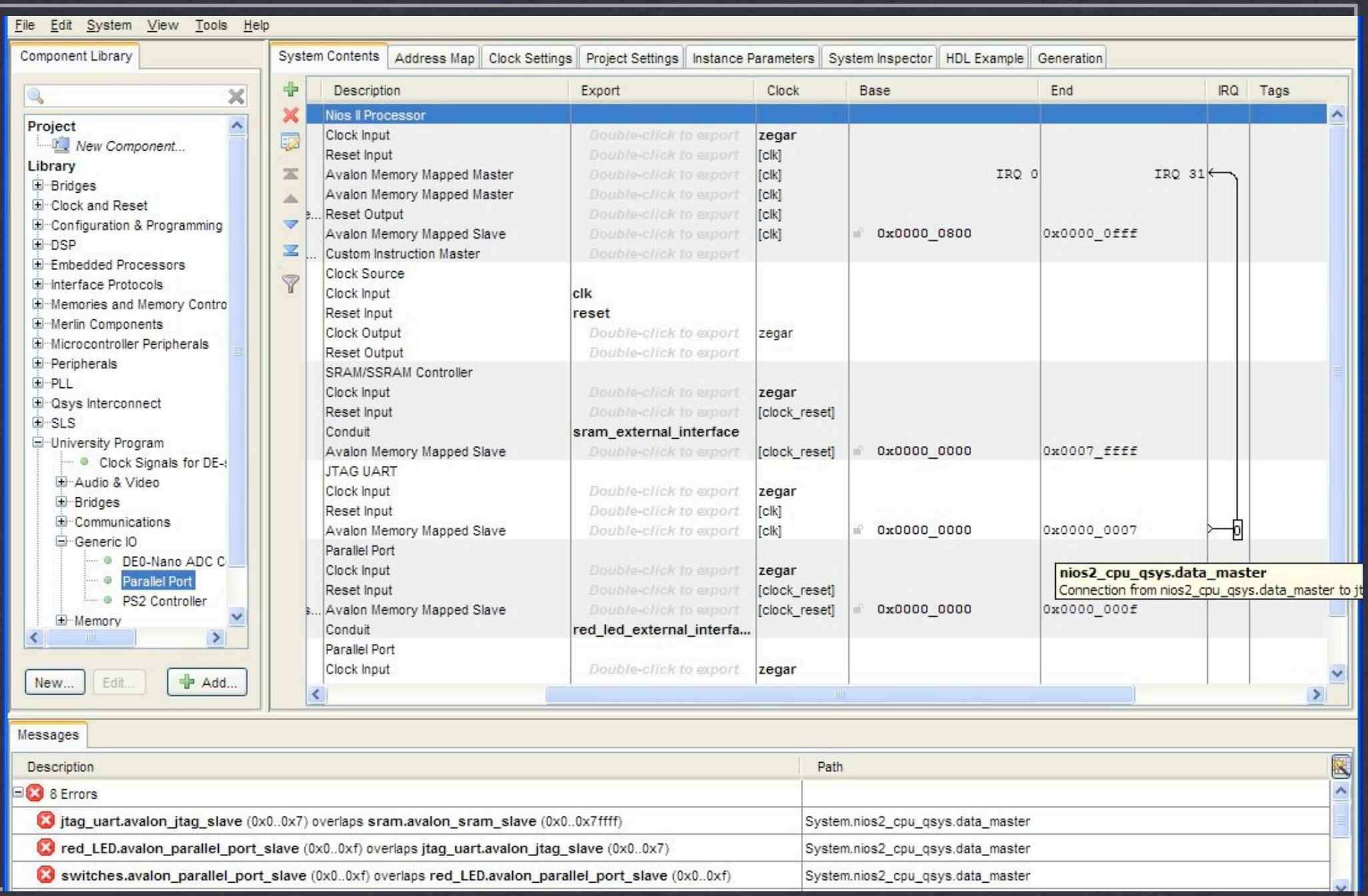

Parallel Port - parallel_port_0
Parallel Port
altera_up_avalon_parallel_port
Documentation
Block Diagram
Show signals
parallel_port_0
clock_reset
clock_reset_reset
avalon_parallel_port_slave
external_interface
clock
reset
avalon
conduit
altera_up_avalon_parallel_port
Configurations
DE-Series Board:
DE2
Create custom parallel port
Presets
I/O device:
Slider Switches
LEDs Colour:
Green
Seven Segment Digits:
3 to 0
Expansion Header:
GPIO 0 (JP1)
Basic Settings (Preset)
Data Width:
18
Port Direction:
Input only
Edge Capture Register
Synchronously Capture
Capture on which edge:
Rising
Generate IRQ
Cancel
Finish


Qsys
File Edit System View Tools Help
Component Library
Project
New Component...
Library
Bridges
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Interface Protocols
Memories and Memory Contro
Merlin Components
Microcontroller Peripherals
Peripherals
PLL
Qsys Interconnect
SLS
University Program
Clock Signals for DE-
Audio & Video
Bridges
Communications
Generic IO
DE0-Nano ADC C
Parallel Port
PS2 Controller
Memory
New...
Edit...
Add...
System Contents
Address Map
Clock Settings
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
Use
Connections
Name
Description
Export
Clock
Base
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
jtag_debug_module_re...
Reset Output
jtag_debug_module
Avalon Memory Mapped Slave
custom_instruction_m...
Custom Instruction Master
zegar
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
zegar
clk_reset
Reset Output
sram
SRAM/SSRAM Controller
clock_reset
Clock Input
zegar
clock_reset_reset
Reset Input
external_interface
Conduit
sram_external_interface
avalon_sram_slave
Avalon Memory Mapped Slave
jtag_uart
JTAG UART
clk
Clock Input
zegar
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
red_LED
Parallel Port
clock_reset
Clock Input
zegar
clock_reset_reset
Reset Input
avalon_parallel_port_s...
Avalon Memory Mapped Slave
external_interface
Conduit
red_led_external_interfa...
switches
Parallel Port
clock_reset
Clock Input
zegar
clock_reset_reset
Reset Input
avalon_parallel_port_s...
Avalon Memory Mapped Slave
external_interface
Conduit
switches_external_interf...
Double-click to export
[clk]
[clock_reset]
0x0000_08
0x0000_00
Messages
Description
Path
12 Errors
"Reset vector memory" (resetSlave) (None) out of range. Valid ranges: [sram.avalon_sram_slave:sram.avalon_sram_s
System.nios2_cpu_qsys
"Exception vector memory" (exceptionSlave) (None) out of range. Valid ranges: [sram.avalon_sram_slave:sram.avalor
System.nios2_cpu_qsys
Reset slave is not specified. Please select the reset slave
System.nios2_cpu_qsys
12 Errors, 1 Warning

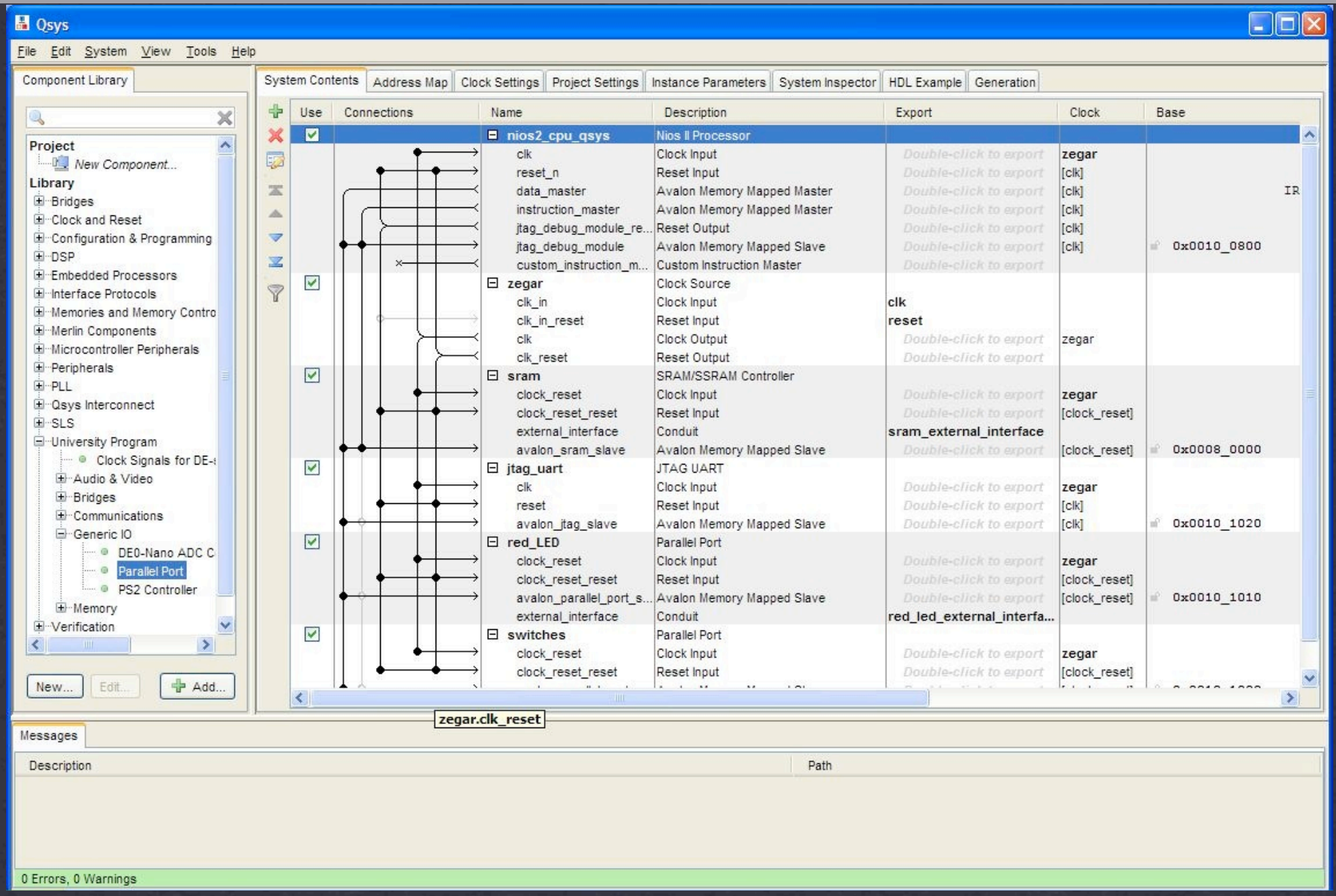


POPRAWA PARAMETRÓW NIOS-A

UZUPEŁNIENIE RESET VECTOR MEMORY I EXCEPTION VECTOR MEMORY

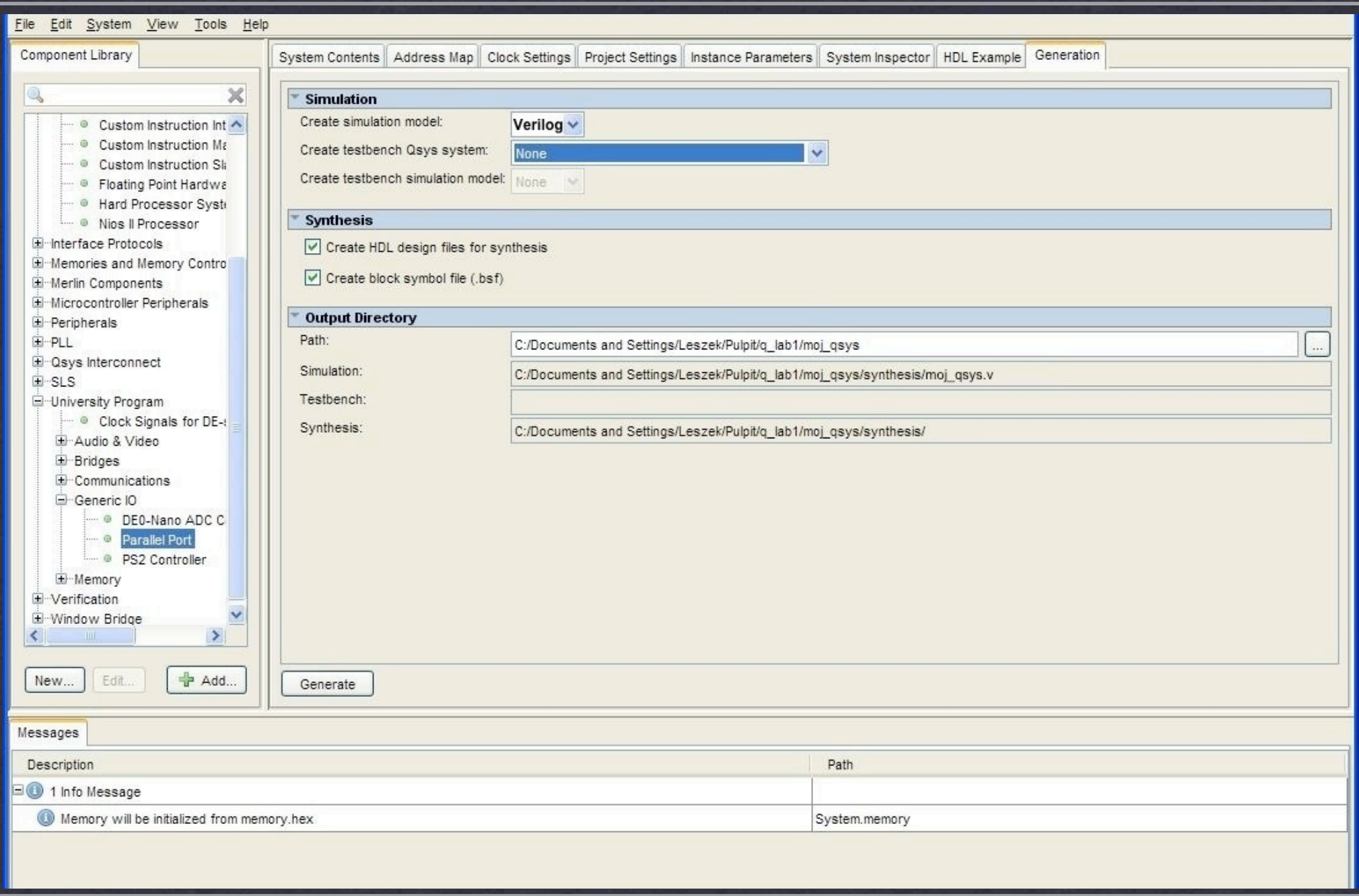


PODŁĄCZAMY SYGNAŁ PRZERWANIA



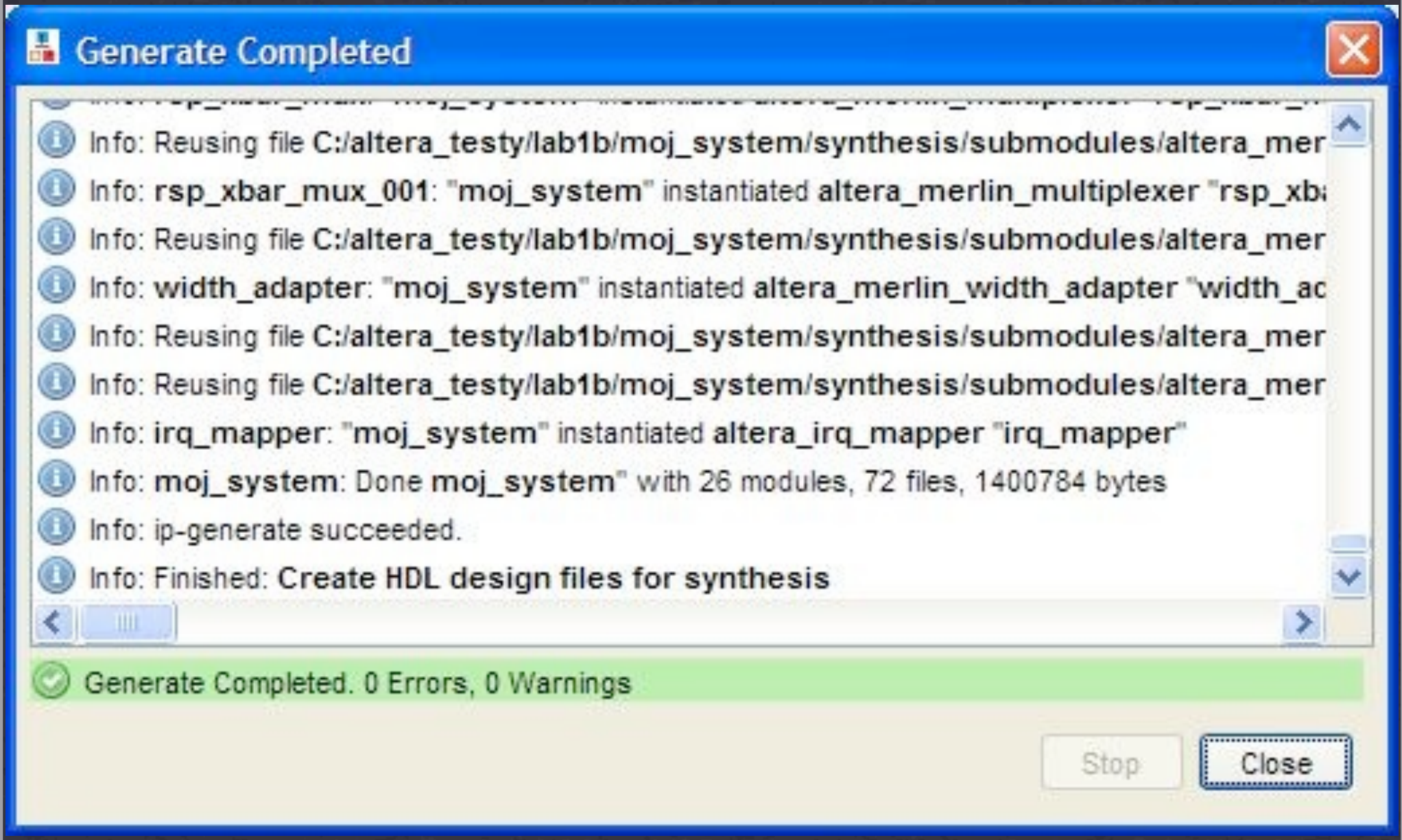
PRZYPISYWANIE ADRESÓW BAZOWYCH

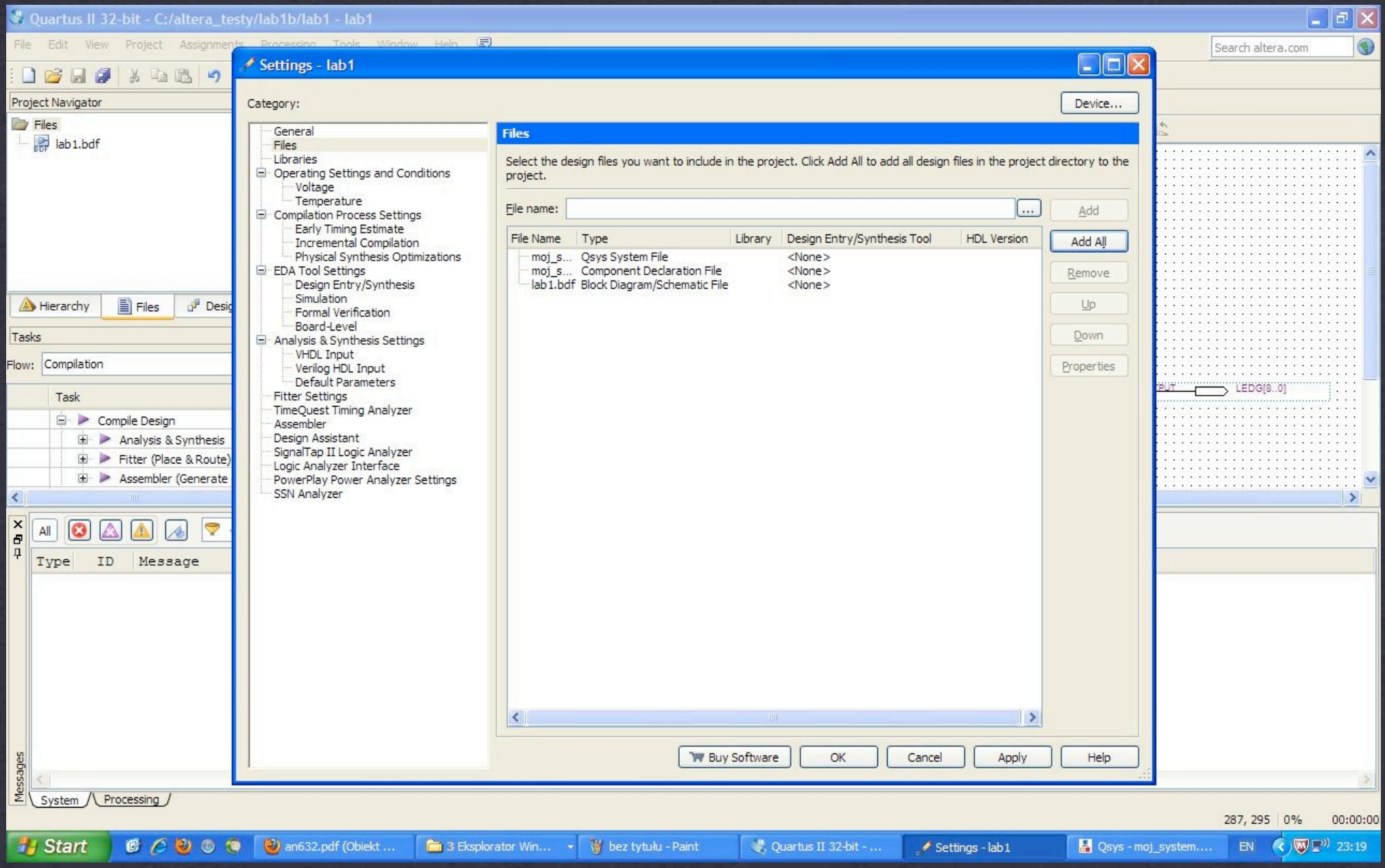
SYSTEM | ASSIGN BASE ADDRESSES



JAKO CREATE SIMULATION MODEL WYBIERAMY VERILOG

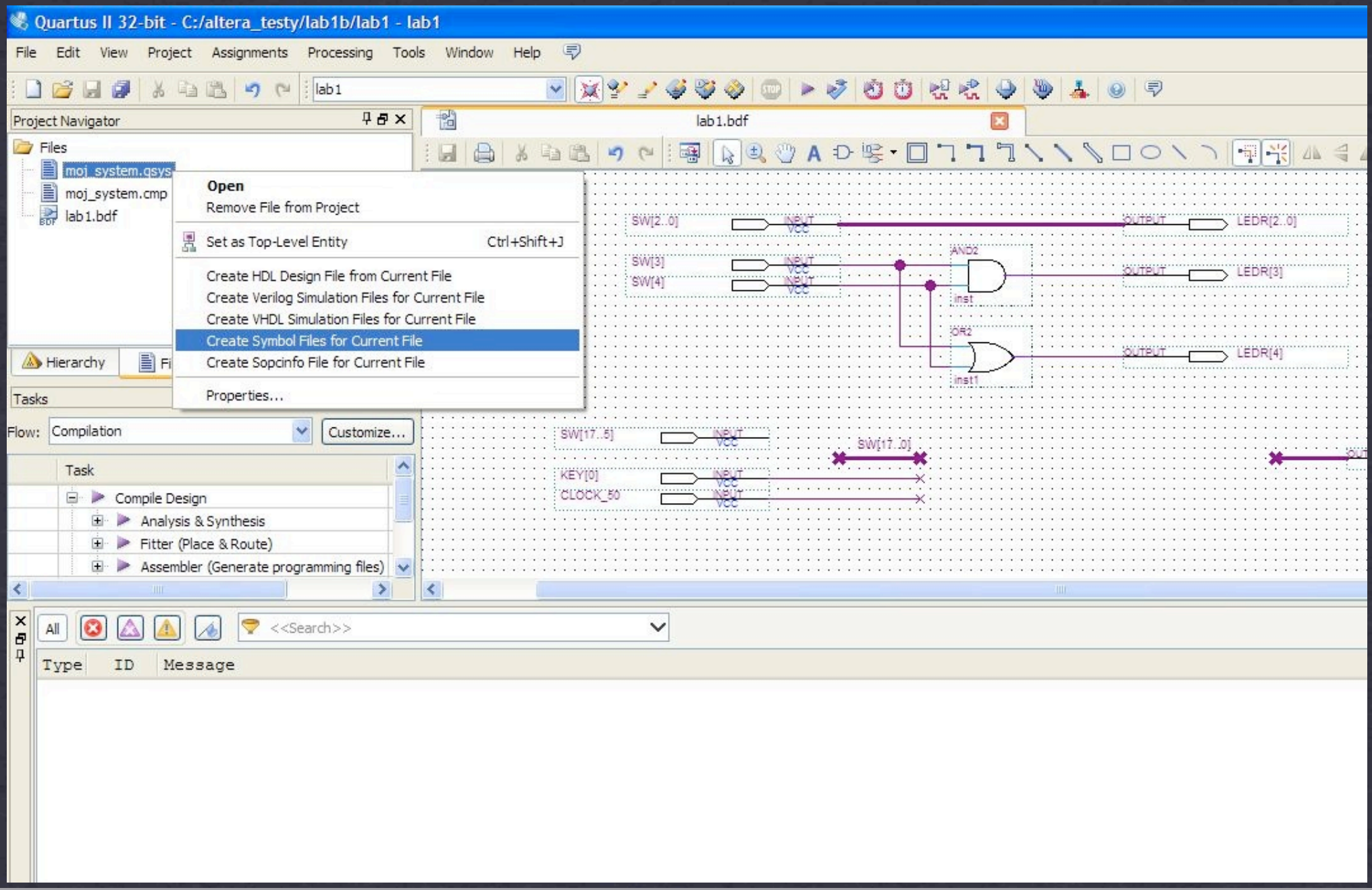
WERSJA VHDL NIE JEST DOPRACOWANA W QUARTUSIE 12.1SP1


Generate Completed
Info: Reusing file C:/altera_testy/lab1b/moj_system/synthesis/submodules/altera_mer
Info: rsp_xbar_mux_001: "moj_system" instantiated altera_merlin_multiplexer "rsp_xb
Info: Reusing file C:/altera_testy/lab1b/moj_system/synthesis/submodules/altera_mer
Info: width_adapter: "moj_system" instantiated altera_merlin_width_adapter "width_ac
Info: Reusing file C:/altera_testy/lab1b/moj_system/synthesis/submodules/altera_mer
Info: Reusing file C:/altera_testy/lab1b/moj_system/synthesis/submodules/altera_mer
Info: irq_mapper: "moj_system" instantiated altera_irq_mapper "irq_mapper"
Info: moj_system: Done moj_system" with 26 modules, 72 files, 1400784 bytes
Info: ip-generate succeeded.
Info: Finished: Create HDL design files for synthesis
Generate Completed. 0 Errors, 0 Warnings
Stop
Close

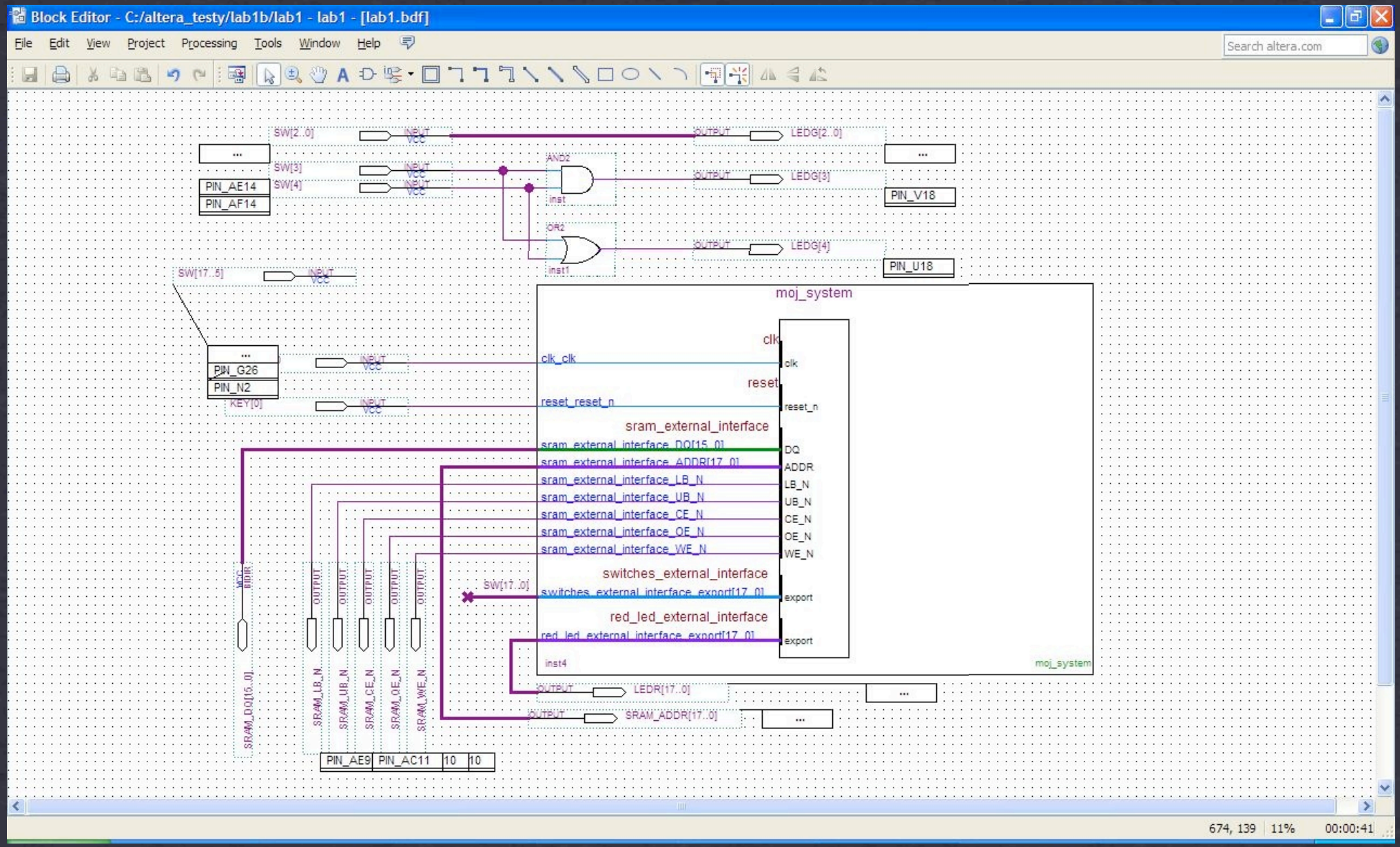


NALEŻY DODAĆ PLIKI NOWEGO PODSYSTEMU

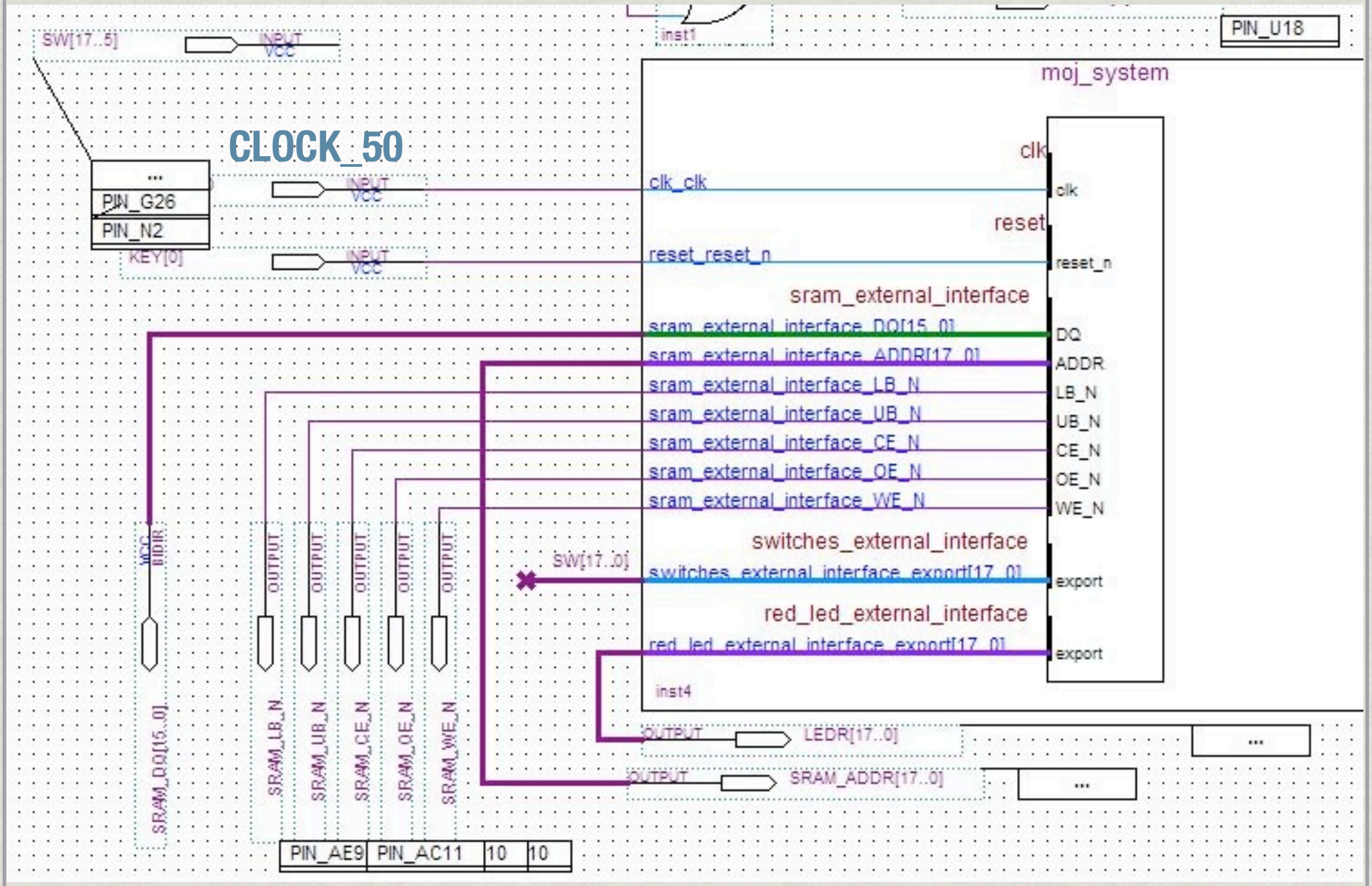
NAJWAŻNIEJSZY JEST PLIK TYPU QSYS SYSTEM FILE



TWORZYMY SYMBOL NOWEGO PODSYSTEMU



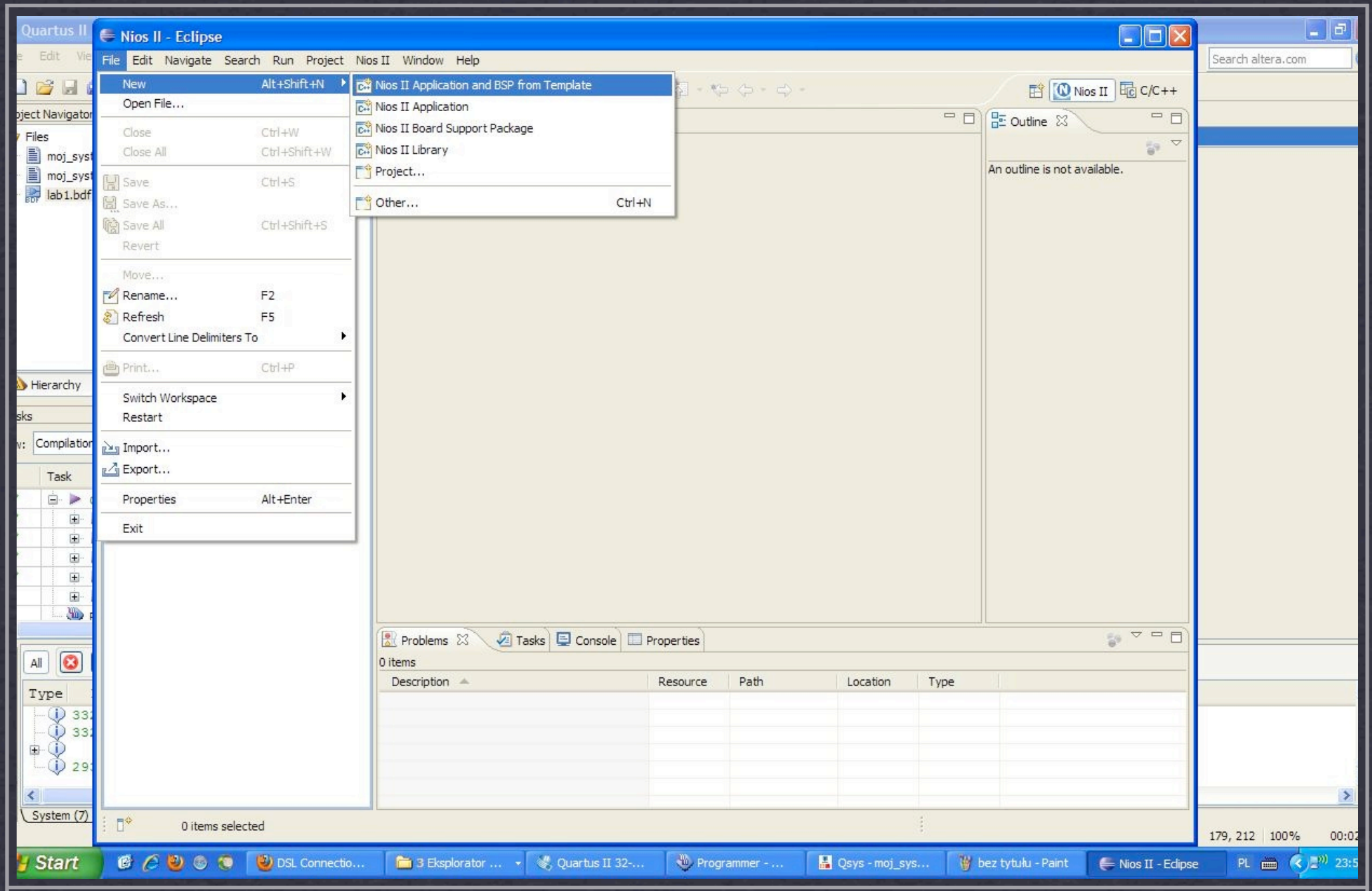
UWAGA: W PODSYSTEMIE WYSTĘPUJĄ: INPUT (WEJŚCIE, NA NIEBIESKO), OUTPUT (WYJŚCIE, NA FIOLETOWO) I BIDIR (DWUKIERUNKOWE, NA ZIELONO)

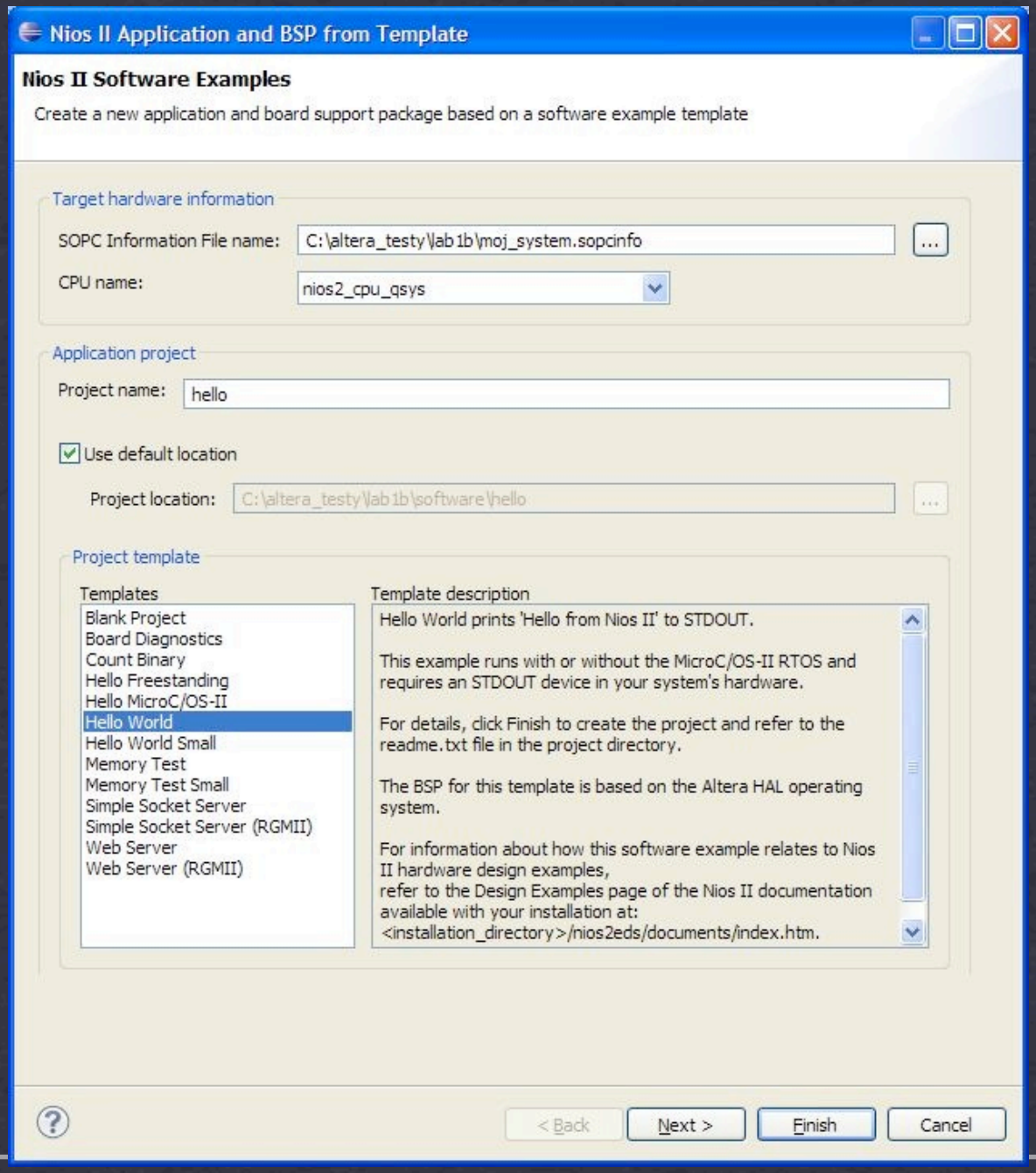

CLOCK_50
moj_system
clk
clk_clk
reset
reset_reset_n
sram_external_interface
sram_external_interface_DQ[15..0]
sram_external_interface_ADDR[17..0]
sram_external_interface_LB_N
sram_external_interface_UB_N
sram_external_interface_CE_N
sram_external_interface_OE_N
sram_external_interface_WE_N
switches_external_interface
switches_external_interface_export[17..0]
red_led_external_interface
red_led_external_interface_export[17..0]
SW[17..0]
SW[17..5]
KEY[0]
PIN_G26
PIN_N2
PIN_U18
LEDR[17..0]
SRAM_ADDR[17..0]
SRAM_DQ[15..0]
SRAM_LB_N
SRAM_UB_N
SRAM_CE_N
SRAM_OE_N
SRAM_WE_N
PIN_AE9
PIN_AC11
inst1
inst4

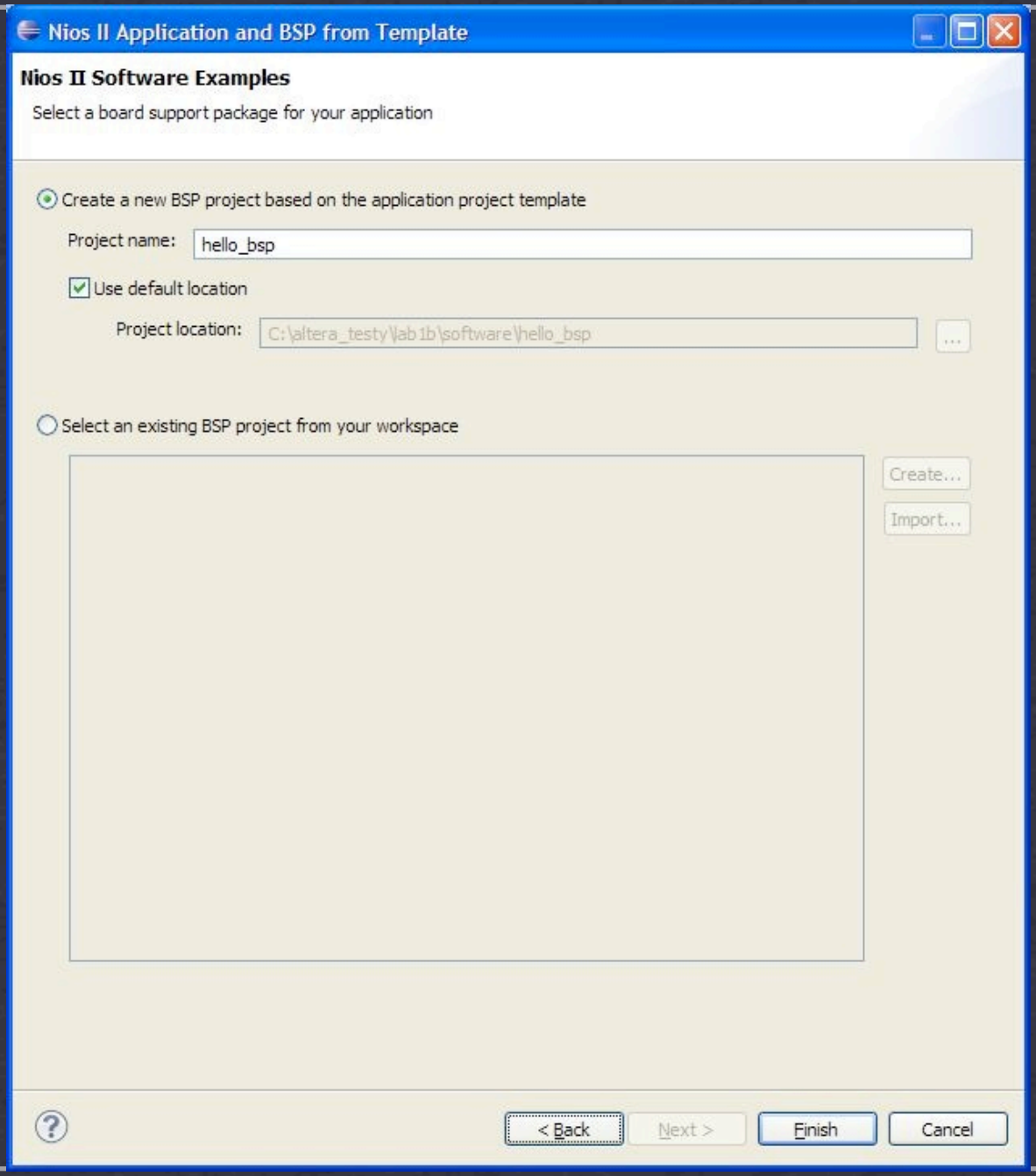
Kolejne kroki

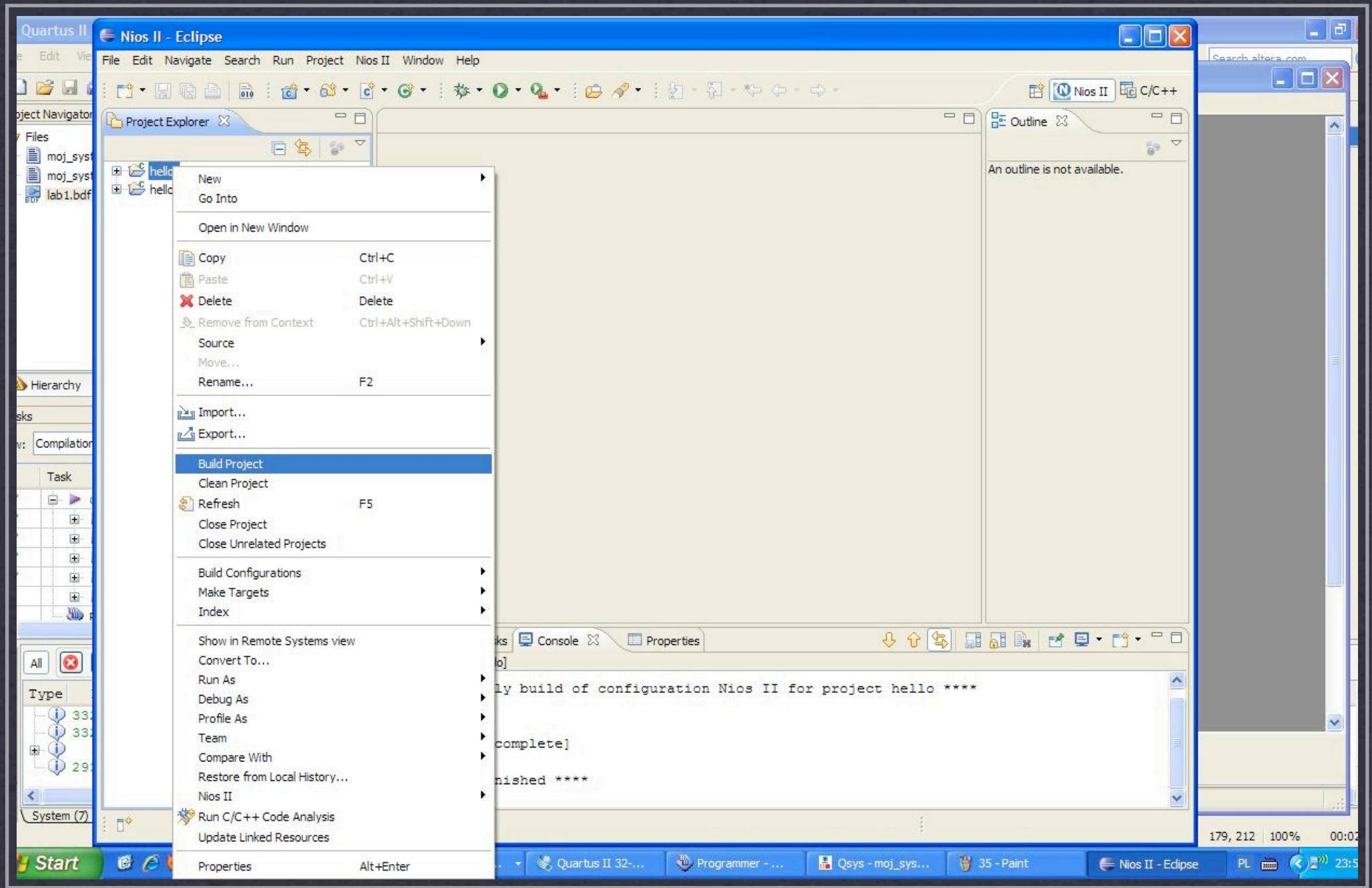
- Wykonać pełną kompilację
- Zaprogramować układ FPGA
- Wybrać polecenie menu Quartusa:
  Tools | Nios II Software Build Tools for Eclipse

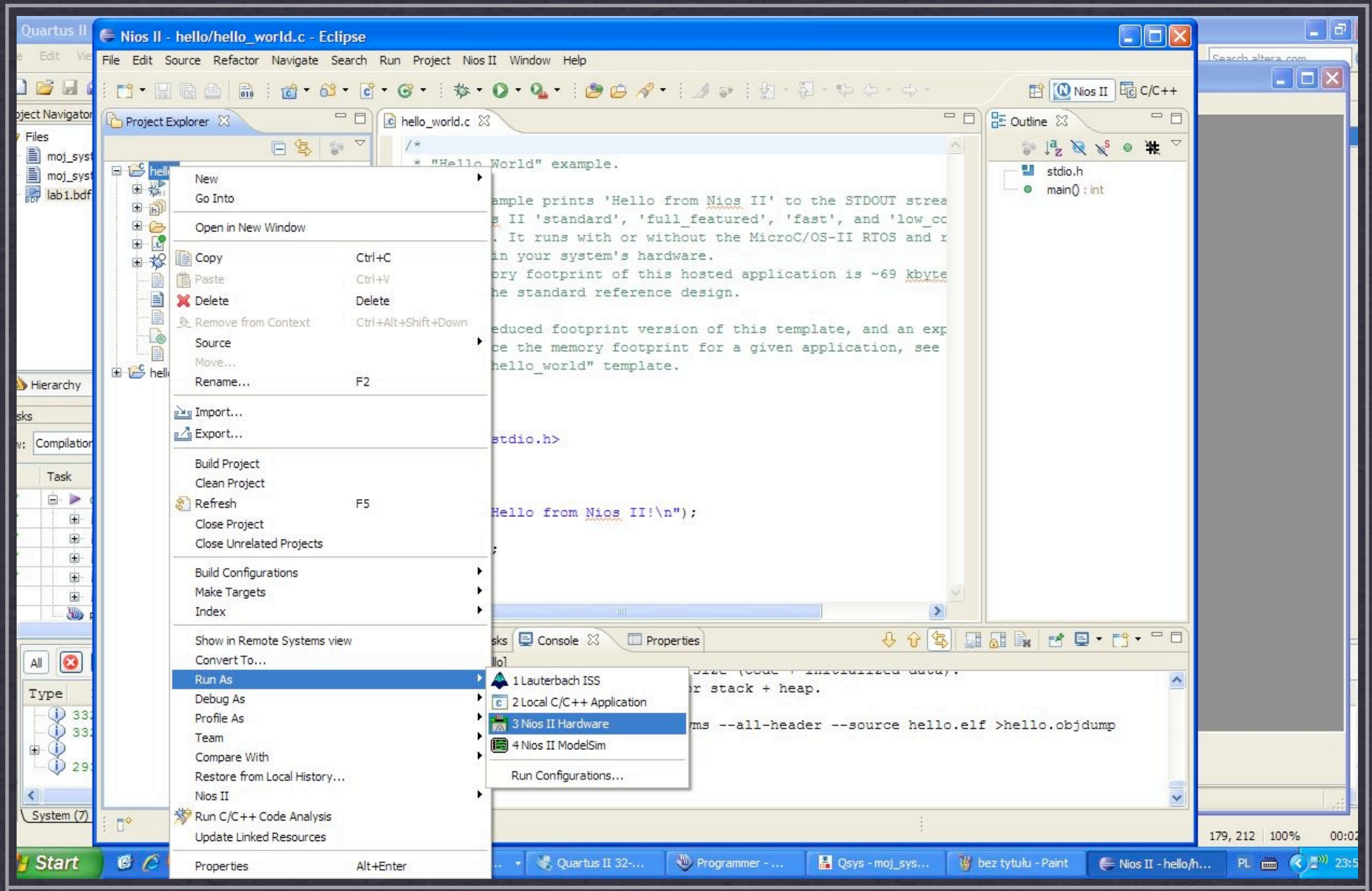
Nios II IDE

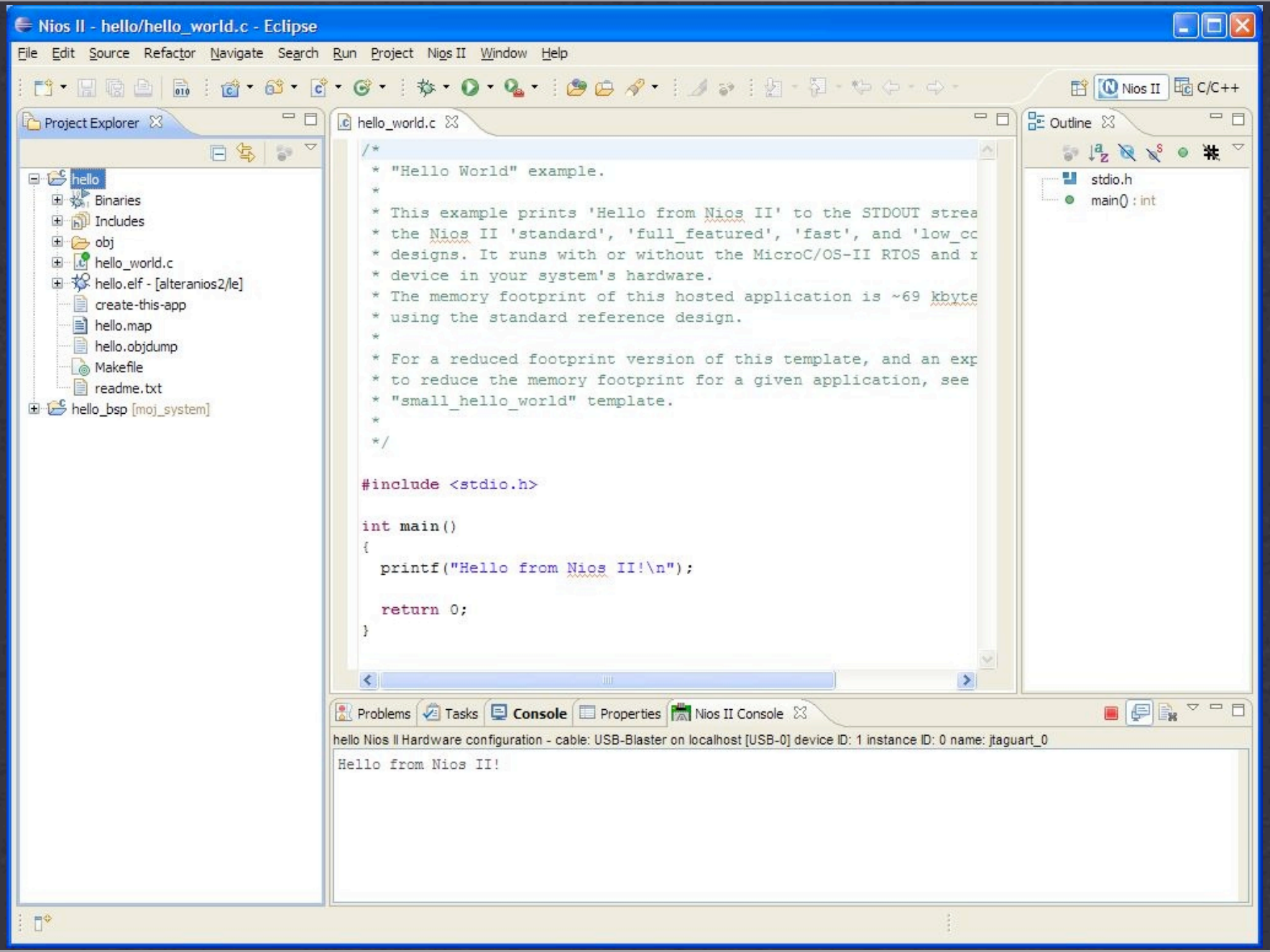

Nios II - Eclipse
File Edit Navigate Search Run Project Nios II Window Help
New Alt+Shift+N
Open File...
Close Ctrl+W
Close All Ctrl+Shift+W
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
Revert
Move...
Rename... F2
Refresh F5
Convert Line Delimiters To
Print... Ctrl+P
Switch Workspace
Restart
Import...
Export...
Properties Alt+Enter
Exit
Nios II Application and BSP from Template
Nios II Application
Nios II Board Support Package
Nios II Library
Project...
Other... Ctrl+N
Nios II
C/C++
Outline
An outline is not available.
Problems
Tasks
Console
Properties
0 items
Description
Resource
Path
Location
Type
0 items selected
Start
DSL Connectio...
3 Eksplorator ...
Quartus II 32-...
Programmer - ...
Qsys - moj_sys...
bez tytułu - Paint
Nios II - Eclipse
PL
179, 212
100%


Nios II Application and BSP from Template
Nios II Software Examples
Create a new application and board support package based on a software example template
Target hardware information
SOPC Information File name:
C:\altera_testy\ab1b\moj_system.sopcinfo
...
CPU name:
nios2_cpu_qsys
Application project
Project name:
hello
Use default location
Project location:
C:\altera_testy\ab1b\software\hello
...
Project template
Templates
Blank Project
Board Diagnostics
Count Binary
Hello Freestanding
Hello MicroC/OS-II
Hello World
Hello World Small
Memory Test
Memory Test Small
Simple Socket Server
Simple Socket Server (RGMII)
Web Server
Web Server (RGMII)
Template description
Hello World prints 'Hello from Nios II' to STDOUT.
This example runs with or without the MicroC/OS-II RTOS and requires an STDOUT device in your system's hardware.
For details, click Finish to create the project and refer to the readme.txt file in the project directory.
The BSP for this template is based on the Altera HAL operating system.
For information about how this software example relates to Nios II hardware design examples,
refer to the Design Examples page of the Nios II documentation available with your installation at:
<installation_directory>/nios2eds/documents/index.htm.
< Back
Next >
Finish
Cancel


Nios II Application and BSP from Template
Nios II Software Examples
Select a board support package for your application
Create a new BSP project based on the application project template
Project name:
hello_bsp
Use default location
Project location:
C:\altera_testy\lab1b\software\hello_bsp
...
Select an existing BSP project from your workspace
Create...
Import...
< Back
Next >
Finish
Cancel


Nios II - Eclipse
File Edit Navigate Search Run Project Nios II Window Help
Project Explorer
Outline
An outline is not available.
New
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
Index
Show in Remote Systems view
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
Nios II
Run C/C++ Code Analysis
Update Linked Resources
Properties Alt+Enter
Console
Properties
ly build of configuration Nios II for project hello ****
complete]
nished ****
Start
Quartus II 32-...
Programmer - ...
Qsys - moj_sys...
35 - Paint
Nios II - Eclipse


Nios II - hello/hello_world.c - Eclipse
File Edit Source Refactor Navigate Search Run Project Nios II Window Help
Project Explorer
hello_world.c
Outline
stdio.h
main() : int
New
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
Index
Show in Remote Systems view
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
Nios II
Run C/C++ Code Analysis
Update Linked Resources
Properties Alt+Enter
1 Lauterbach ISS
2 Local C/C++ Application
3 Nios II Hardware
4 Nios II ModelSim
Run Configurations...
Console
Properties
Start

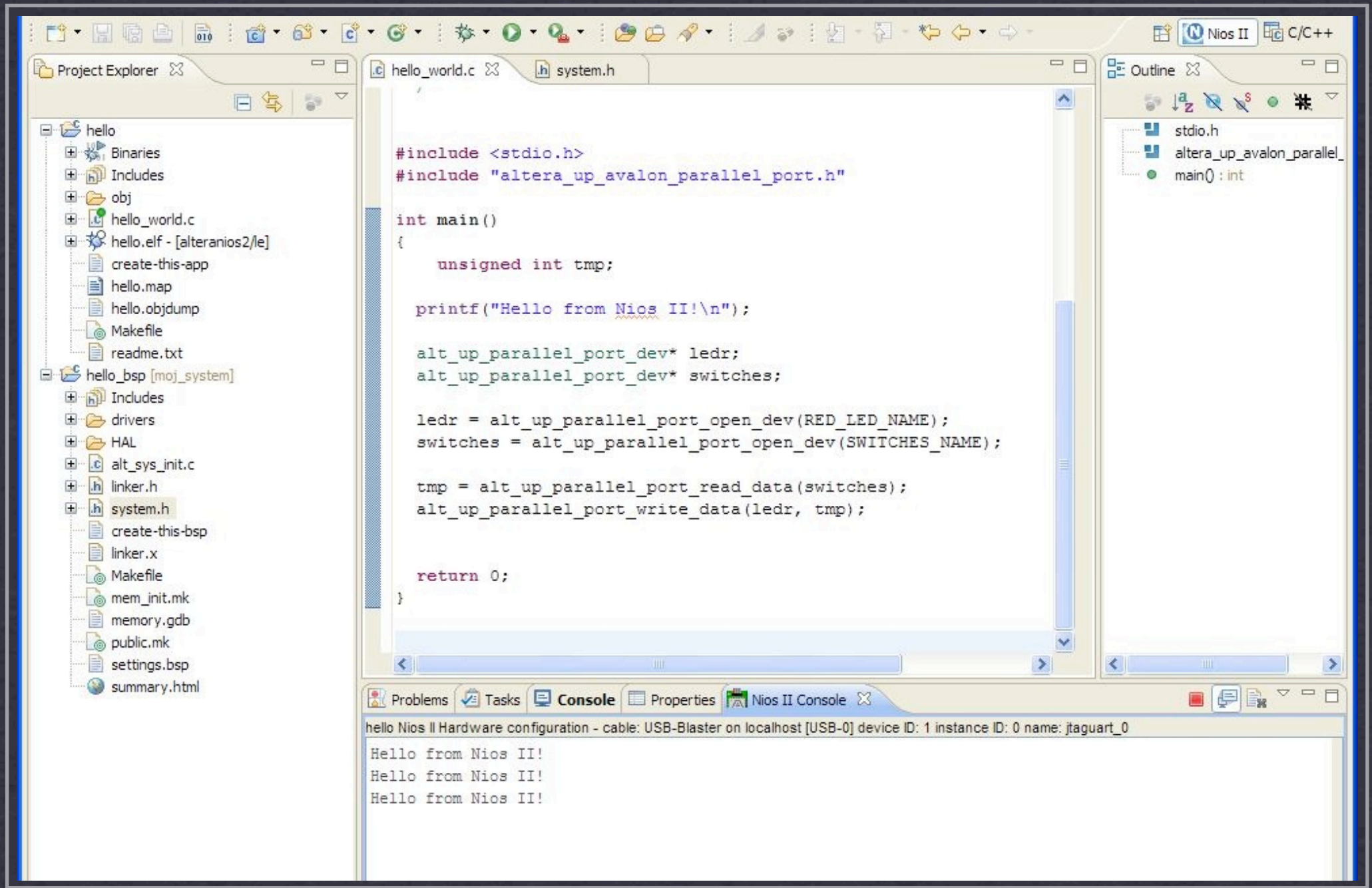

Nios II - hello/hello_world.c - Eclipse
File Edit Source Refactor Navigate Search Run Project Nios II Window Help
Nios II
C/C++
Project Explorer
hello
Binaries
Includes
obj
hello_world.c
hello.elf - [alteranios2/le]
create-this-app
hello.map
hello.objdump
Makefile
readme.txt
hello_bsp [moj_system]
hello_world.c
/*
* "Hello World" example.
*
* This example prints 'Hello from Nios II' to the STDOUT strea
* the Nios II 'standard', 'full_featured', 'fast', and 'low_co
* designs. It runs with or without the MicroC/OS-II RTOS and r
* device in your system's hardware.
* The memory footprint of this hosted application is ~69 kbyte
* using the standard reference design.
*
* For a reduced footprint version of this template, and an exp
* to reduce the memory footprint for a given application, see
* "small_hello_world" template.
*
*/
#include <stdio.h>
int main()
{
printf("Hello from Nios II!\n");
return 0;
}
Outline
stdio.h
main() : int
Problems
Tasks
Console
Properties
Nios II Console
hello Nios II Hardware configuration - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtaguart_0
Hello from Nios II!

Dodajemy kod

- alt_up_parallel_port_dev* ledr;
- alt_up_parallel_port_dev* switches;

- ledr = alt_up_parallel_port_open_dev (RED_LED_NAME);
- switches = alt_up_parallel_port_open_dev (SWITCHES_NAME);

- tmp = alt_up_parallel_port_read_data(switches);
- alt_up_parallel_port_write_data(ledr, tmp);



ZIELONE DIODY ZMIENIAJĄ KOLOR NA BIEŻĄCO

CZERWONE DIODY ZMIENIAJĄ KOLOR PO WCIŚNIĘCIU GUZIKA KEY0

Koniec