lpm_rom (ROM)

Parameterized ROM Megafunction

Altera recommends that you use the `lpm_rom` function to implement all ROM functions. The `lpm_rom` function is available only for ACEX 1k and FLEX 10K devices.

The MAX+PLUS II Compiler automatically implements suitable portions of this function in EABs in ACEX 1K and FLEX 10K devices. Therefore, it is not necessary to use the *Implement in EAB* logic option for this function, and doing so may cause warning messages to appear.

Altera also recommends instantiating this function as described in Creating a Custom Megafunction Variation with the MegaWizard Plug-In Manager.

You can use the **genmem** utility to create a simulation model for this function for use in third-party simulators. Type `genmem -h` ↵ at a DOS or UNIX prompt for information on how to use this utility.

AHDL Function Prototype (port name and order also apply to Verilog HDL):

```
FUNCTION lpm_rom (address[LPM_WIDTHAD-1..0], inclock, outclock, memenab)
   WITH (LPM_WIDTH, LPM_WIDTHAD, LPM_NUMWORDS, LPM_FILE, LPM_ADDRESS_CONTROL, LPM_OUTDATA)
   RETURNS (q[LPM_WIDTH-1..0]);
```

VHDL Component Declaration:

```
COMPONENT lpm_rom
   GENERIC (LPM_WIDTH: POSITIVE;
      LPM_TYPE: STRING := "LPM_ROM";
      LPM_WIDTHAD: POSITIVE;
      LPM_NUMWORDS: NATURAL := 0;
      LPM_FILE: STRING;
      LPM_ADDRESS_CONTROL: STRING := "REGISTERED";
      LPM_OUTDATA: STRING := "REGISTERED";
      LPM_HINT: STRING := "UNUSED");
   PORT (address: IN STD_LOGIC_VECTOR(LPM_WIDTHAD-1 DOWNTO 0);
      inclock: IN STD_LOGIC := '0';
      outclock: IN STD_LOGIC := '0';
      memenab: IN STD_LOGIC := '1';
      q: OUT STD_LOGIC_VECTOR(LPM_WIDTH-1 DOWNTO 0));
END COMPONENT;
```

Ports:

INPUTS

Port Name	Required	Description	Comments
`address[]`	Yes	Address input to the memory.	Input port `LPM_WIDTHAD` wide.
`inclock`	No	Clock for input registers.	The `address[]` port is synchronous (registered) when the `inclock` port is connected, and is asynchronous (unregistered) when the `inclock` port is not connected.
`outclock`	No	Clock for output registers.	The addressed memory content-to-`q[]` response is synchronous when the `outclock` port is connected, and is asynchronous when it is not connected.
`memenab`	No	Memory enable input.	High = data output on `q[]`, Low = high-impedance outputs

OUTPUTS

Port Name	Required	Description	Comments
`q[]`	Yes	Output of memory.	Output port `LPM_WIDTH` wide.

Parameters:

Parameter	Type	Required	Description

LPM_WIDTH	Integer	Yes	Width of the q[] port.
LPM_WIDTHAD	Integer	Yes	Width of the address[] port. LPM_WIDTHAD should be (but is not required to be) equal to LOG2(LPM_NUMWORDS). If LPM_WIDTHAD is too small, some memory locations will not be addressable. If it is too large, the addresses that are too high will return undefined logic levels.
LPM_NUMWORDS	Integer	No	Number of words stored in memory. In general, this value should be (but is not required to be) 2 ^ LPM_WIDTHAD-1 < LPM_NUMWORDS <= 2 ^ LPM_WIDTHAD. If omitted, the default is 2 ^ LPM_WIDTHAD.
LPM_FILE	String	Yes	Name of the Memory Initialization File (.mif) or Hexadecimal (Intel-Format) File (.hex) containing ROM initialization data ("*<filename>*"), or "UNUSED".
LPM_ADDRESS_CONTROL	String	No	Values are "REGISTERED", "UNREGISTERED", and "UNUSED". Indicates whether the address port is registered. If omitted, the default is "REGISTERED".
LPM_OUTDATA	String	No	Values are "REGISTERED", "UNREGISTERED", and "UNUSED". Indicates whether the q and eq ports are registered. If omitted, the default is "REGISTERED".
LPM_HINT	String	No	Allows you to specify Altera-specific parameters in VHDL Design Files. The default is "UNUSED".
LPM_TYPE	String	No	Identifies the LPM entity name in VHDL Design Files.

Function:

Synchronous Read from Memory

OUTCLOCK	MEMENAB	Function
X	L	q[] output is high impedance (memory not enabled).
not ~	H	No change in output.
~	H	The output register is loaded with the contents of the memory location pointed to by address[]. q[] outputs the contents of the output register.

Asynchronous Memory Operations

Totally asynchronous memory operations occur when neither inclock nor outclock is connected. The output q[] is asynchronous and reflects the data in the memory to which address[] points.

MEMENAB	Function *Note 1*
L	q[] output is high-impedance (memory not enabled).
H	The memory location pointed to by address[] is read.

Resource Usage:

Uses one embedded cell per memory bit.

See also:

- Implementing RAM & ROM (AHDL)
- Implementing RAM & ROM (VHDL)
- Implementing RAM & ROM (Verilog HDL)
- Initializing RAM or ROM
- Megafunctions/LPM