//First draft

Evaluation of the project implemented in Digital/Quartus:
Stage I: design of the instruction set, data path, and microinstructions – maximum 60 points,
Stage II: design of the simplified control unit and instruction fetch unit – maximum 25 points,
Stage III: design of the complete control unit and memory manager; implementation and simulation of the developed CPU components and execution of a sample processor program using Digital or Quartus II – 15 points.

To receive points for Stage II, the elements associated with Stage I must be designed correctly. Similarly, to receive points for Stage III, the elements associated with Stage II must be designed correctly. In Stage III, the CPU design MUST compile without errors in Digital / Quartus II, and a representative program performing calculations on the CPU must be prepared (the program should be provided as a MIF file within the project).

Evaluation of the project implemented as a software simulation:
Stage I: design of the instruction set and microinstructions, logic implementing data path functions – maximum 60 points,
Stage II: implementation of the CPU and memory simulator (including a simplified GUI) – maximum 25 points,
Stage III: implementation of the complete simulator including a sample application – 15 points.
To receive points for Stage II, the elements associated with Stage I must be designed correctly. Similarly, to receive points for Stage III, the elements associated with Stage II must be designed correctly.